Curriculum vitæ
Iulian OBER

Last updated on February 2, 2018

Contact

Address
IRIT, Universite de Toulouse
118 route de Narbonne
31062 Toulouse, France

Phone: +33 5 61 55 6339

E-mail: iulian.ober@irit.fr
Web: http://www.irit.fr/~Iulian.Ober/

Education & Degrees

2010 : *Habilitation à Diriger des Recherches (HDR) University of Toulouse.*
Title : Observer pour vérifier, contraindre et interagir. Applications de l'observation à la construction et à la validation des systèmes logiciels
Reviewers : Prof. Yves LEDRU, Université Joseph Fourier, Grenoble, France
Prof. Elie NAJM, Telecom ParisTech, Paris, France
Prof. Dorina PETRIU, Carleton University, Ottawa, Canada
Habilitation defended on December 13th, 2010.

2001 : *Ph.D. in Computer Science and Telecommunications*, Institut National Polytechnique de Toulouse - École Nationale Supérieure d'Électronique, Électrotechnique, Informatique, d'Hydraulique et de Télécommunications de Toulouse (ENSEEIHT).
Title : Specification and Validation of Timed Systems with Formal Description Languages
Advisor : Prof. Bernard COULETTE
Reviewers : M. Joseph SIFAKIS, CNRS/Verimag
M. Roland GROZ, CNET
Thesis defended on September 21st, 2001. Mention: "Très honorable".

1998 : *M.Sc. in Computer Science, Babeş – Bolyai University of Cluj, Romania.*
Title : Design and implementation of a back-end for a UML/OCL CASE tool.
Thesis prepared while in internship at Vérilog (Toulouse, France).
Class rank: 1st.

1997 : *B.Sc. in Mathematics and Computer science*, Babeş – Bolyai University of Cluj, Romania. Class rank: 1st.

Academic and other research positions

2005 - today : **Associate Professor ("Maître de conférences", tenured)** – University of Toulouse, Technology Institute of Blagnac. Member of IRIT - a public research laboratory of CNRS and the University of Toulouse. **Main responsibilities**:

- **Jan. 2013 - July 2015** : Head of the MACAO (Models, Architectures, Components, Agility and prOcesses) research team at IRIT. The team was composed of 3 Full Professors and 9 Associate Professors.
- **Sep. 2011 - Sep. 2017** : Deputy head of the Master's Degree Program "Collaborative Software Engineering", responsible for the 1st year. University of Toulouse (professional/alternating, 20 to 25 students per year).

2011 (spring semester) : **Visiting Associate Professor** at the Institute for Software Integrated Systems, Vanderbilt University (USA), during a research leave (teaching sabbatical) granted by the French National Universities Council (CNU).

2003 - 2005 : **Researcher** – Verimag. Verimag is a public research laboratory of CNRS, Joseph Fourier University of Grenoble and Grenoble INP.

2002 - 2003 : **Post-doctoral fellow** – Verimag laboratory.

1998 - 2001 : **R&D engineer**, Vérilog S.A. / Télélogic A.B., Toulouse (while Ph.D. candidate).

1995 - 1998 : **Research Assistant**, Computer Science Laboratory, Babeş – Bolyai University of Cluj, Romania (while undergraduate and Masters student).

Research focus

Blending formal specifications and verification techniques with widely used, industry-grade model-based design methods for real-time embedded and cyber-physical systems. This includes:

- Applying formal verification (mainly model-checking) in model-based software and systems engineering
- Contract-based design of real-time components and systems
- Improving the usability of simulation and model-checking results based on domain and model-specific information.

Published work

See full list lists at:
. https://www.irit.fr/-Publications-?code=4601&nom=Ober+Iulian
and almost full ones at:
. http://dblp.uni-trier.de/pers/hd/o/Ober:Iulian.html
. https://scholar.google.com/citations?user=Q81KjzYAAAAJ
Some of my most relevant / cited publications are listed below:

[1] Marius Bozga, Susanne Graf, Ileana Ober, Iulian Ober, and Joseph Sifakis. The IF Toolset. In Marco Bernardo and Flavio Corradini, editors, *Formal Methods for the Design of Real-Time Systems, International School on Formal Methods for the Design of Computer, Communication and Software Systems, SFM-RT 2004, Bertinoro, Italy, September 13-18, 2004, Revised Lectures*, volume 3185 of *LNCS*, pages 237–267. Springer, 2004.

[2] Iulian Ober, Susanne Graf, and Ileana Ober. Validating timed UML models by simulation and verification. *International Journal on Software Tools for Technology Transfer*, 8(2):128–145, 2006.

[3] Josef Hooman, Hillel Kugler, Iulian Ober, Angelika Votintseva, and Yuri Yushtein. Supporting UML-based Development of Embedded Systems by Formal Techniques. *Software and Systems Modeling*, 7(2):131–155, 2008.

[4] Iulia Dragomir, Iulian Ober, and Christian Percebois. Contract-based modeling and verification of timed safety requirements within SysML. *Software and Systems Modeling*, 16(2):587–624, mai 2017.

Projects and grants

2016-2019 : Bombardier Transportation Grant
Description of work: Bombardier Transportation aims to develop a fully integrated and tool-supported methodology for the system design of railway transport systems. Parts of this method are already in use but lack uniformity of semantics and of usage of models at the different stages, as well as support for the use of models during software-in-the-loop and hardware-in-the-loop design validation phases. The grant project aims to bridge these gaps and achieve a fully integrated method.
Role: co-leader (with Prof. JM Bruel, IRIT)

2009-2011 : European Space Agency Project 22618/09/NL/JK "FullMDE : Full Model Driven Development for On-Board Software"
Partners : Astrium Space Transportation, Esterel Technologies, IRIT, Verimag, Praxis
Description of work: adaptation of the Omega modeling and validation methods to system level models in SysML.
Role: leader of the IRIT team.

2008-2011 : SoCKET - French DGE Project "System on Chip Toolkit For Critical Embedded Systems")
Partners: 20 partners from academia and industry. Leader: ST Microelectronics.
Overall project goal: integration of model driven techniques in the design flow of systems-on-chip (SoC). Contribution: support and case studies on using Omega SysML for the modeling and validation of SoC designs.

2008-2010 : European Space Agency Activity 3-12639 "OMEGA2"
Partners : IRIT, Verimag
Description of work: upgrading the Omega modeling and validation platform for UML version

2.x and support for integrating the platform in ESA's operational environment.
Role: leader

2004-2007 : National Research Agency (ANR) Project RNTL-PERSIFORM "Performance engineering based on simulation of formal functional models"
Partners: France Telecom R&D, Verimag, Institut National des Télécommunications (INT), IRISA, Orpheus. Description of work: integration of performance modeling and evaluation in a development process, by extension of functional modeling languages (UML activity diagrams) and bridging with queuing networks models and languages (HyPerformix).
Role: leader of the Verimag team.

2004-2007 : ASSERT - EU Integrated Project IST "Automated proof based System and Software Engineering for Real-Time Systems"
Partners: 26 partners from academia and industry. Leader: European Space Agency (ESA) Contribution: Study and semantics definition of the ASSERT modeling language. Alignment between ASSERT models and Omega UML, tool integration.

2002-2005 : OMEGA - EU Project IST "Correct Development of Real-Time Embedded Systems in UML"
Partenaires: Verimag (leader), France Telecom R&D, EADS, Israel Aircraft Industries, NLR, Université de Kiel, Universit de de Nijmegen, Weizmann Institute of Science, OFFIS, Centrum Wiskunde en Informatica (CWI).
Contribution: Definition of a UML profile for real-time critical systems (Omega UML). Definition of semantics. Design and implementation of simulation and model checking tools. Application on industry case studies from partners Astrium, NLR and IAI.

2000-2002 : INTERVAL - EU Project IST "Formal Design, Validation and Testing of Real-Time Telecommunications Systems"
Partners: Ericsson, Telelogic, Teletel, Solinet, Verimag, France Telecom R&D.
Contribution: Timed constraints definition framework for the SDL language. Extension of the Telelogic ObjectGeode tool to timed verification and test-case generation.

Program committees

- Workshop committee, STAF 2018 (co-chair)
- International System Design Languages Forum (SDL) : 2011 (PC co-chair), 2013, 2015, 2017
- International Workshop on Model-Based Verification and Validation : 2016
- International Workshop on Model-based Architecting of Cyber-Physical and Embedded Systems : 2015 (chair)
- International Workshop on Model Based Architecting and Construction of Embedded Systems (ACES-MB) : 2008-2014 (PC and steering committee)
- Asia-Pacific Software Engineering Conference (APSEC) : 2011 - 2014
- System Analysis and Modelling Workshop (SAM) : 2012 - 2018

- International Conference on Ambient Systems, Networks and Technologies (ANT) : 2012, 2013
- Workshop on Model-Based Verification and Validation: From Research to Practice (MVV) : 2012
- ACM/IEEE International Conference on Model Driven Engineering Languages and Systems (MODELS) : 2010
- International Workshop on the Certification of Safety-Critical Software Controlled Systems (SafeCert) : 2008 - 2010
- MODELS Doctoral Symposium 2009,
- MODELS Research Project Symposium 2008 (chair)
- International Workshop on Modeling and Analysis of Real-Time Embedded Systems (MARTES), 2005, 2006

Invited talks, contributions, tutorials

- Invited talk at the Modelling Wizards School organized in connection with MODELS 2012, Innsbruck, October, 2012
- Invited talk at ETR (Ecole Temps Réel) Summerschool 2009, Télécom ParisTech, September, 2009
- Invited talk at Dagstuhl Seminar 09361 on Design and Validation of Concurrent Systems, September, 2009
- Chapter in monograph *Modeling and Verification of Real-time Systems*, Stephan Merz, Nicolas Navet (ed.), John Wiley & Sons, 2008
- Invited talk at Dagstuhl Seminar 07241 on Tools for the Model-based Development of Certifiable Systems, June, 2007
- Chapter in monograph *Systèmes Temps Réel: Techniques de description et de vérification*, Nicolas Navet (ed.), Hermès, 2006
- Invited lecture "Modeling of Real-Time Systems with SDL and UML", University of Applied Science, Hagenberg, Austria, 2005
- Tutorials on "IF: A Validation Environment for Real-time UML and SDL Models", at 12th International Conference on System Design Languages (SDL Forum, Copenhagen, 2005) and 11th International SPIN Workshop on Model Checking of Software (Barcelona, 2004)

Ph.D. students

- Younes Lakhrissi (graduated in July, 2010) – co-advisor: B. Coulette
  Subject: Integration of behavior models in view-based analysis and design.
- Hong-Viet Luong (graduated in October, 2010) – co-advisors: C. Percebois, A-L. Courbis, T. Lambolais
  Subject: Incremental construction and verification of system specifications.
- El Arbi Abussoror (graduated in September, 2013) co-advisor: Ileana Ober
  Subject: Advanced diagnostic methods in formal model validation.
- Iulia Dragomir (graduated in December, 2014) co-advisor: C. Percebois
  Subject: Contract-based modeling and verification of timed safety requirements for system design in SysML.

- Ronan Baduel (started in 2016) co-advisor: J-M. Bruel
  Subject: An integrated model-based early validation approach for Railway Systems.
  Financed by a grant from Bombardier Transportation.

Other academic service activities

2007 - 2011 and 2014 - 2017 : Elected member of the "Comité Scientifique Qualifié" (permanent committee appointing the faculty recruitment commissions) in Computer Science at Toulouse 2 University

2013 - 2015 : Member of the scientific council of IRIT.

2012 - 2015 : Elected member of the board ("Conseil de laboratoire"), IRIT laboratory.