

Tightness and Computation Assessment of Worst-Case Delay Bounds in Wormhole Networks-On-Chip

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Outline

Problem Statement

BATA

Tightness Analysis

Computation Analysis

Case Study

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Network-on-chip (NoC)

- ▶ Widely used and scalable interconnect for manycore platforms and SoCs

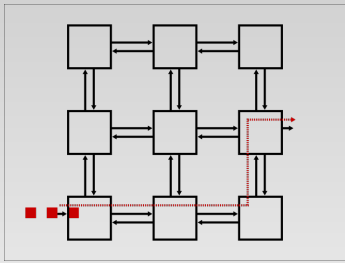
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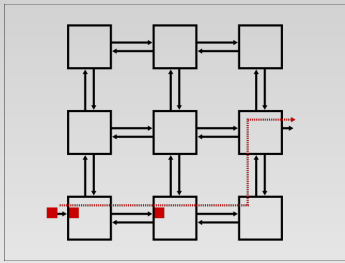
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- ▶ Low latency, high throughput
- ▶ Wormhole Routing allows small buffer sizes

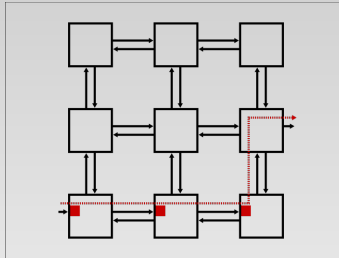
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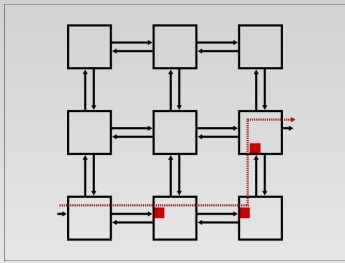
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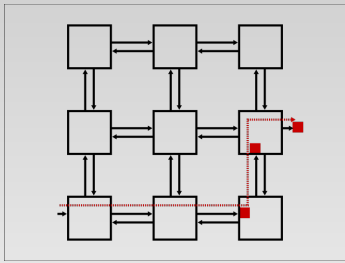
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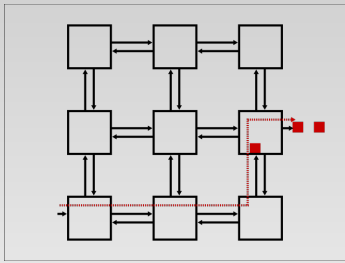
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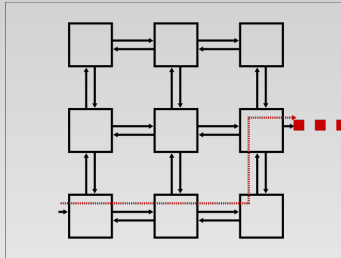
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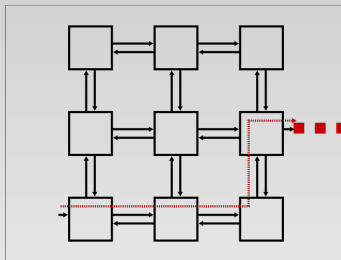
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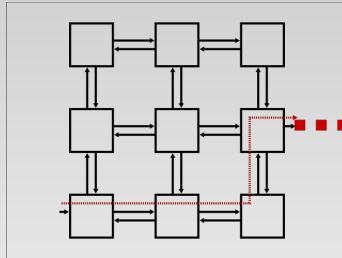


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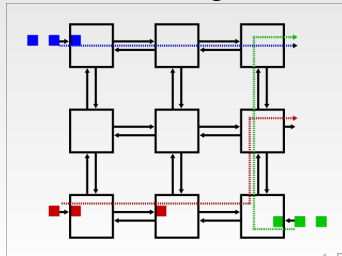


Now with congestion :

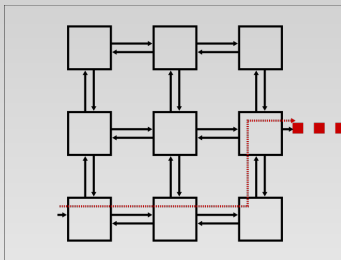
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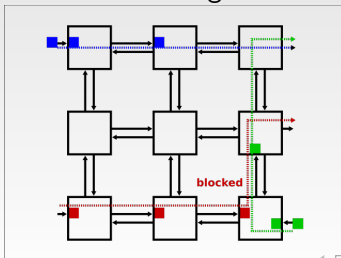
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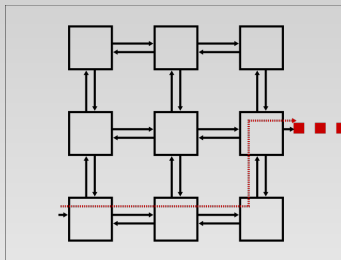
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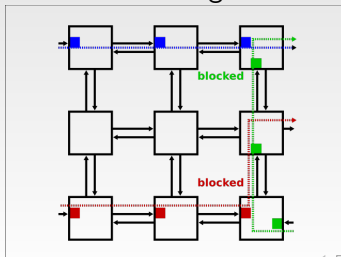
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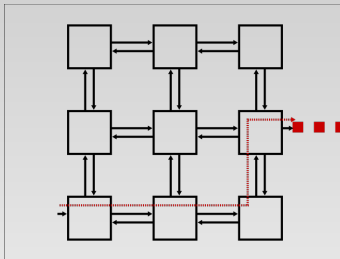
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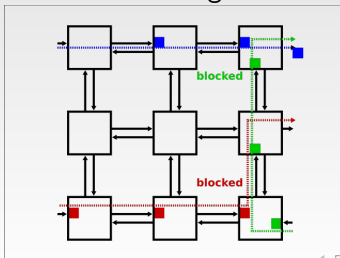
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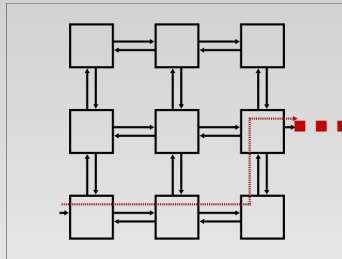
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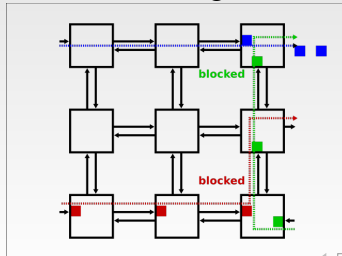
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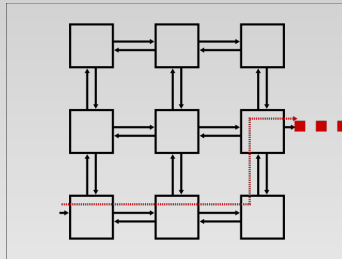
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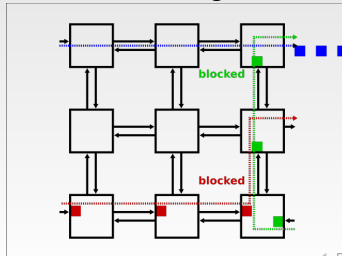
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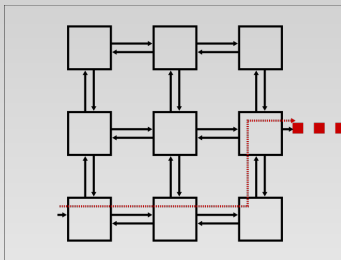
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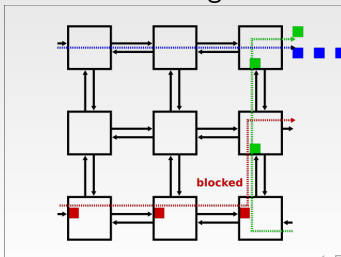
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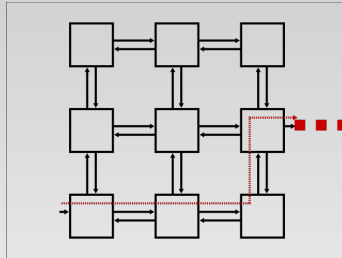
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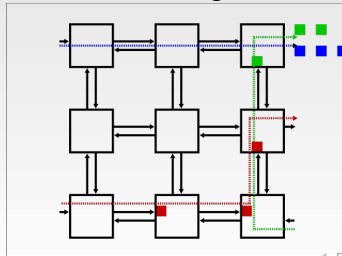
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Challenges of wormhole

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- ▶ Flows that do not share resources may interfere (**indirect blocking**)

Main existing approaches

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- ▶ **Network Calculus**: KTH [8, 9, 10], **our approach BATA [11]**

Approach Contribution	ST				CPA		RC			NC			BATA[11]	
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wormhole	x	x	x	x	x	x	x	x	x	x		x	x	x
multiple VCs	x	x	x	x		x						x	x	x
priority sharing		x	x		x	x					x	x		x
VCs sharing						x								x
flows serialization				x		x			x		x	x		x
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Based on **Network Calculus**:

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- ▶ provide a general and tight approach

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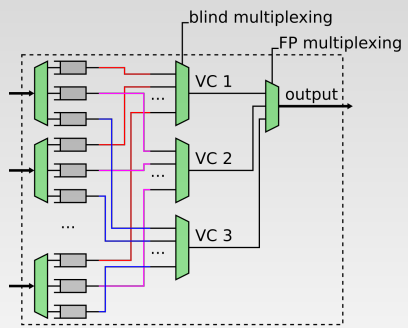
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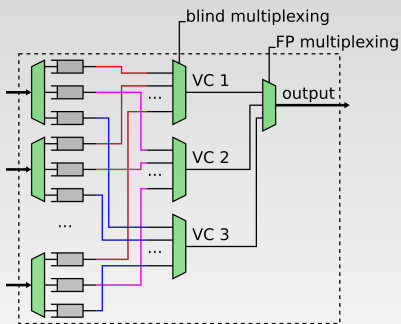
Case Study

System Model and Assumptions

- ▶ **Input-buffered routers**
(minor changes for output-buffered routers)

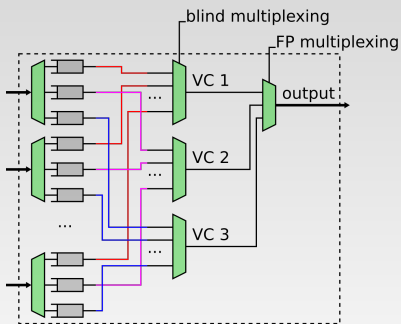


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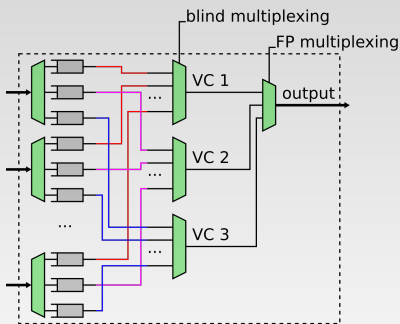
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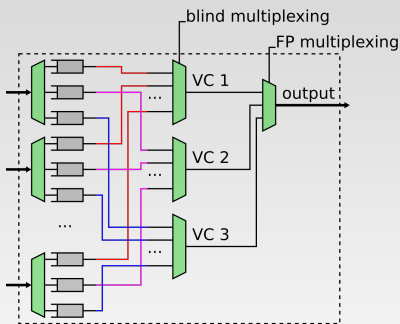
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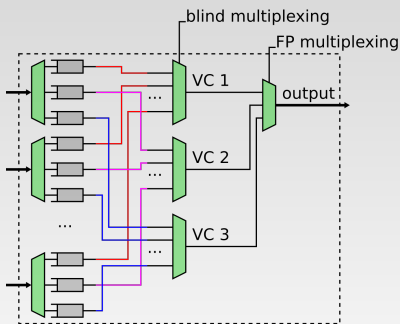
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Direct blocking latency, due to flows sharing resources with f

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Technological latency (routers)

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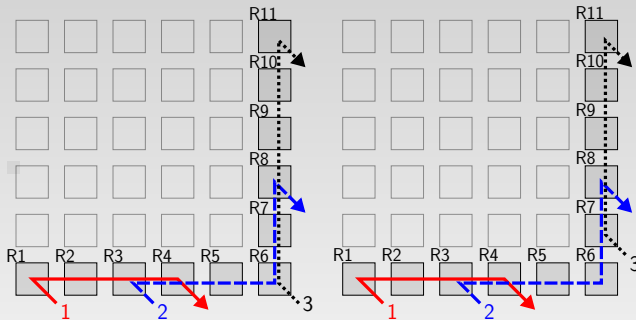
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Indirect blocking latency, due to backpressure: takes buffer size into account

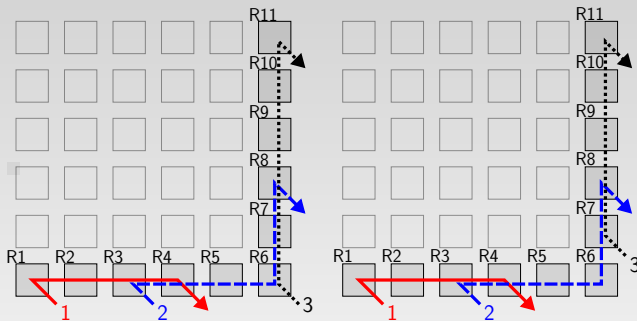
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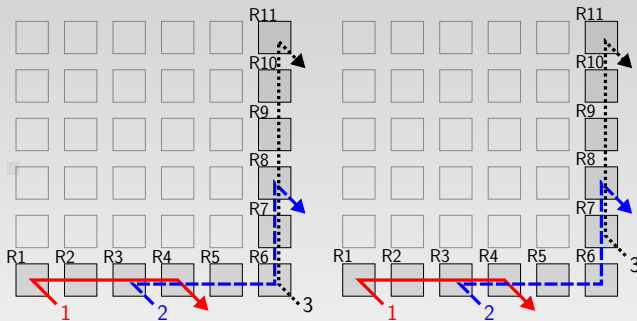
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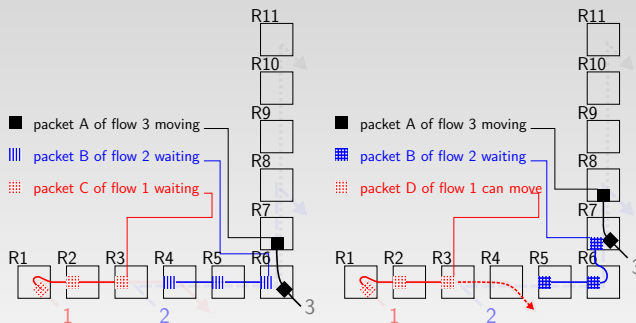
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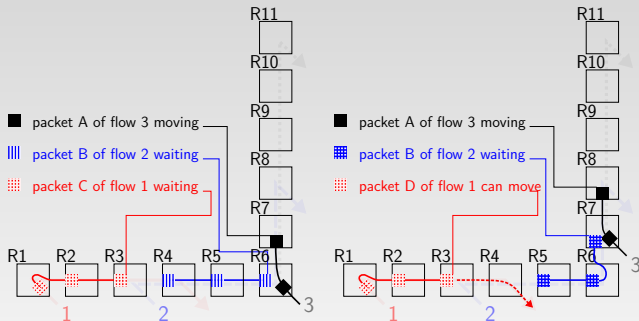
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Flow 3 blocks flow 1 in only one configuration!

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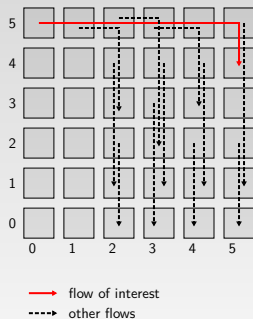
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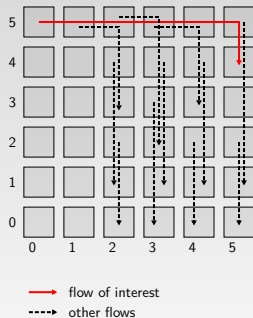
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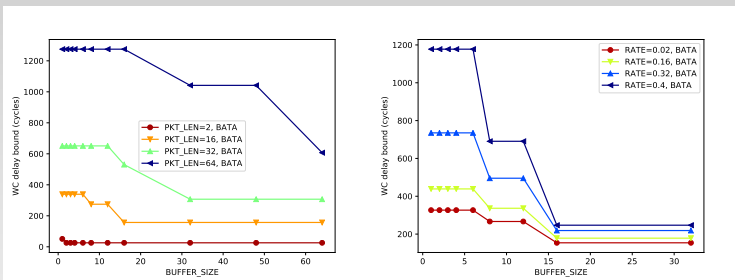
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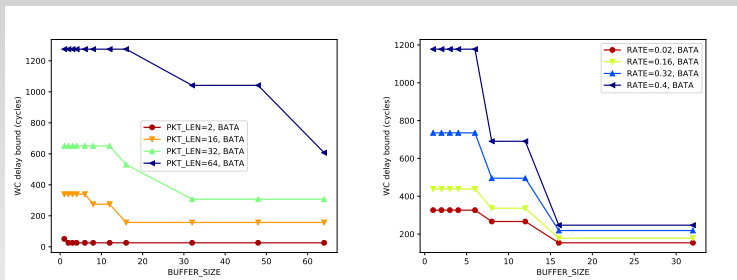


We use a configuration exhibiting a lot of potential interference between flows

Results

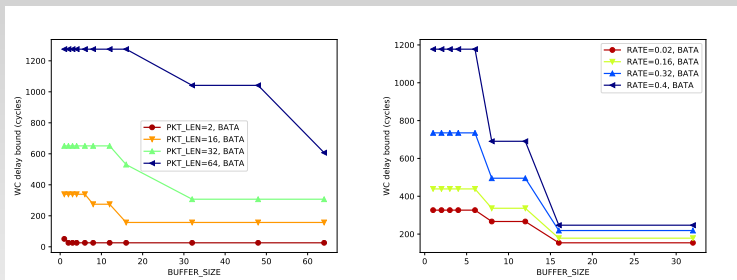


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“Step decrease” of delay bounds when $B \nearrow$

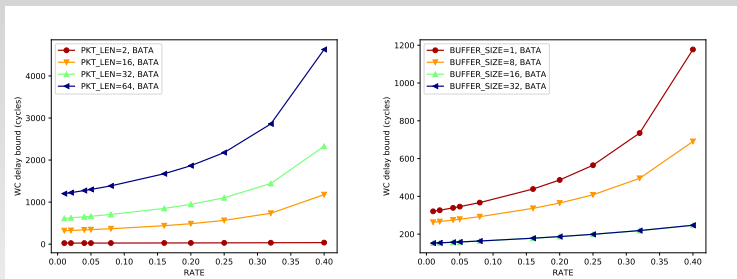
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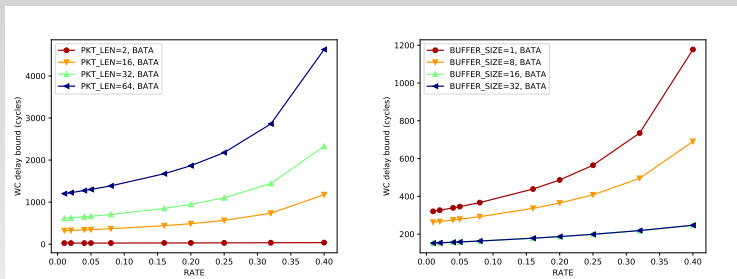
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Buffer size: directly impacts spread index and complexity of IB patterns

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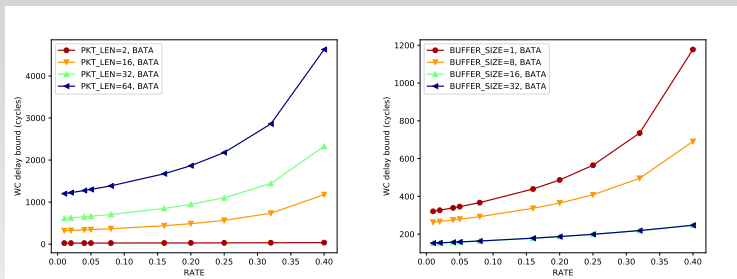


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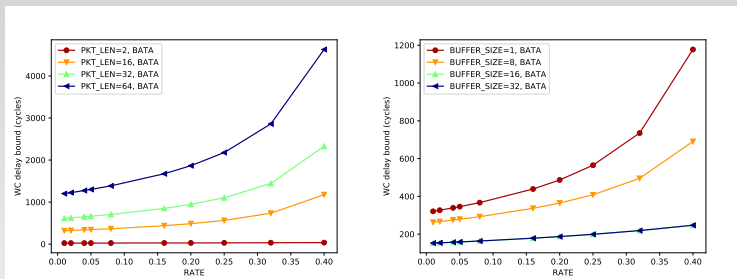
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We perform the tightness analysis while varying **buffer size** and **flow rate**

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Buffer	4	8	16	4	8	16

Tightness Statistics

Average	70.1%	72.1%	80.8%	49.7%	64.2%	79.8%
Max	91.7%	92.0%	88.3%	95.6%	88.9%	97.3%
Min	40.6%	38.1%	48.9%	20.8%	33.3%	43.8%

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- ▶ Average tightness up to 80%

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Compute **tightness ratio** $\tau = \frac{\text{Simulated worst-case}}{\text{Theoretical bound}}$

→ **lower bound** of the actual tightness!

Rate	8%			32%		
Buffer	4	8	16	4	8	16

Tightness Statistics

Average	70.1%	72.1%	80.8%	49.7%	64.2%	79.8%
Max	91.7%	92.0%	88.3%	95.6%	88.9%	97.3%
Min	40.6%	38.1%	48.9%	20.8%	33.3%	43.8%

Results

- ▶ Average tightness up to 80%
- ▶ Tightness is better for large buffers and small rates

Outline

Problem Statement

BATA

Tightness Analysis

Computation Analysis

Case Study

Computational Analysis

Goal

Determine how well the approach scales

Computational Analysis

Goal

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Method

- ▶ Use many randomly generated configurations with different numbers of flows (4 to 128)

Computational Analysis

Goal

Determine how well the approach scales

Method

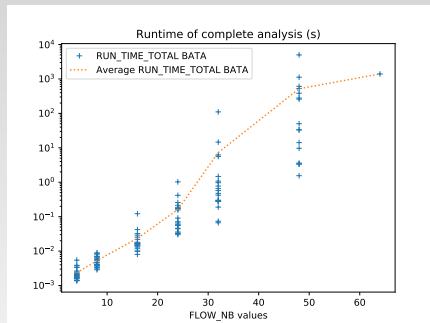
- ▶ Use many randomly generated configurations with different numbers of flows (4 to 128)
- ▶ Perform timing analysis and measure the computation times (total, IB analysis, service curve computation)

Results

Complete analysis

Results

Complete analysis

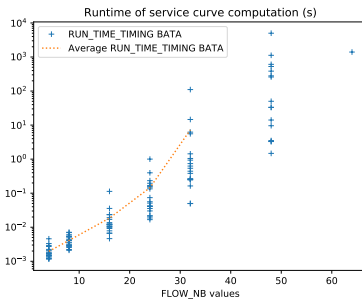
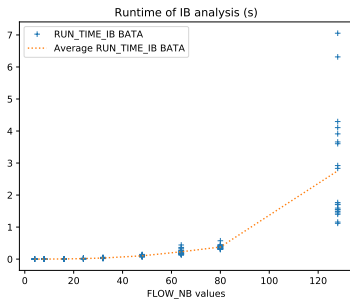


Results

Split IB analysis and service curve computation

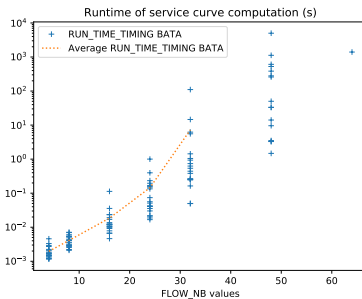
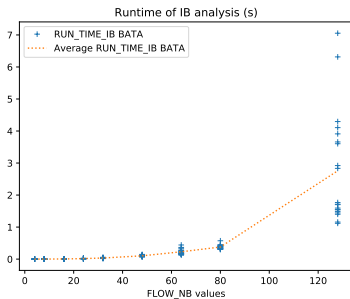
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Complexity: **service curve computation**

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Control of an autonomous vehicle, used in [12]

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- ▶ 4×4 manycore chip with a mesh-NoC

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Computations for **different buffer sizes** (2, 100 flits and infinite)

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Analysis

Computations for **different buffer sizes** (2, 100 flits and infinite)
Comparison with state-of-the-art approach [12] based on ST
Further computations with **shared VCs**

Comparative Results

Delay bounds and simulated delays

	$B = 2$	$B = 100$	$B = \infty$
Average tightness	64%	67%	71%
Average tightness difference	+0.07%	+0.08%	-0.03%
Maximum tightness difference	+3.70%	+3.49%	+0.01%
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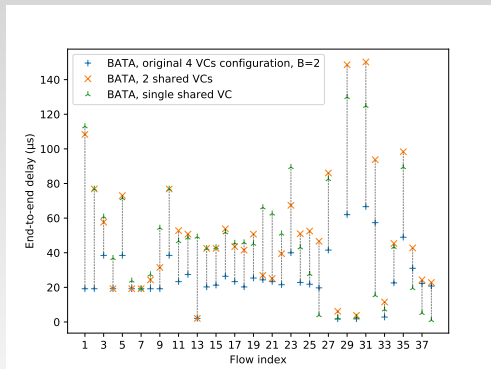
- ▶ Delay bounds are **very similar** to [12]
- ▶ On average, they differ by less than 0.1%
- ▶ **Good tightness**: 64% to 71% on average

Extended Results

We reduced the number of VCs and computed the WC bounds

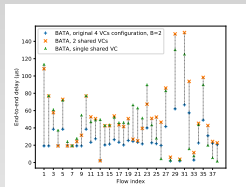
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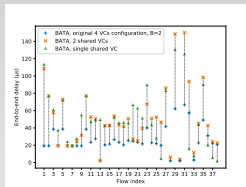


Improvements of BATA

- ▶ All flows remain schedulable with 2 shared VCs

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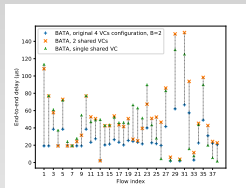


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- ▶ All flows remain schedulable with 2 shared VCs
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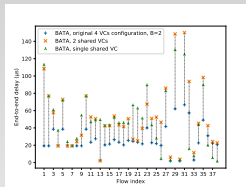


Improvements of BATA

- ▶ All flows remain schedulable with 2 shared VCs
- ▶ All flows remain schedulable with one shared VC
- ▶ Wider applicability domain

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Improvements of BATA

- ▶ All flows remain schedulable with 2 shared VCs
- ▶ All flows remain schedulable with one shared VC
- ▶ Wider applicability domain
- ▶ Computation times with shared VCs are higher but remain reasonable

Summary

BATA is:

- ▶ **generic** (multiple shared VCs, priority-sharing, buffer size. . .)

Summary

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Summary

BATA is:

- ▶ **generic** (multiple shared VCs, priority-sharing, buffer size...)
- ▶ **tight**
- ▶ ...but **computationally expensive!**

Perspectives

- ▶ **Computational aspect:** reduce complexity of the approach





Perspectives




- ▶ **Computational aspect**: reduce complexity of the approach
- ▶ **Applicability**: extend model to support bursty traffic on heterogeneous platforms





Perspectives




- ▶ **Computational aspect**: reduce complexity of the approach
- ▶ **Applicability**: extend model to support bursty traffic on heterogeneous platforms
- ▶ **Integration** : integrate model in DSE methodologies

Thank you for your attention!

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