VILESCO TECHNOLOGIES

REAL TIME CHALLENGES IN ENGINE CONTROL SYSTEMS

RTNS'2019 27TH INTERNATIONAL CONFERENCE ON REAL-TIME NETWORKS AND SYSTEM

ENSEEIHT Toulouse, 06.11.2019 Denis Claraz – Vitesco Technologies France S.A.S.

Public

REAL TIME ENGINE CONTROL CHALLENGES

1 INDUSTRIAL CONSTRAINTS

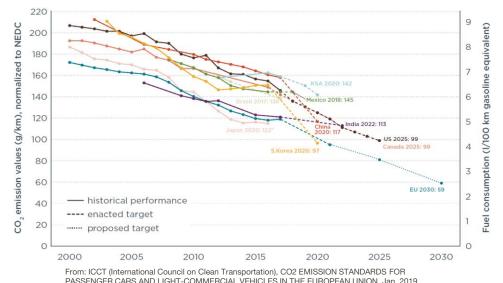
2 TECHNICAL CONSTRAINTS

3 CONCLUSION

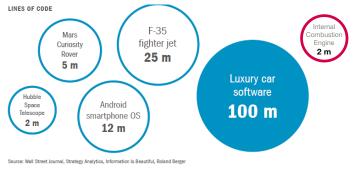


INTERNAL COMBUSTION ENGINE (ICE) SYSTEM OVERVIEW

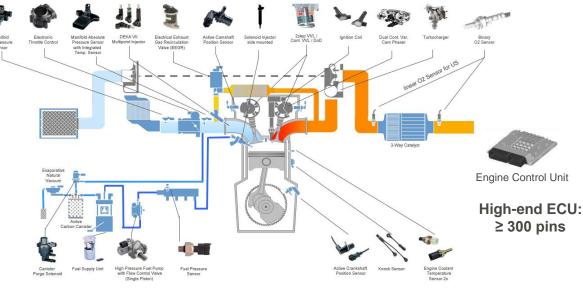
MAIN MARKET DRIVER IS EMISSION REDUCTION



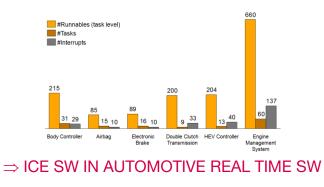
GLOBAL WARMING \Rightarrow CO2 EMISSION REDUCTION







 \Rightarrow INCREASE COMPLEXITY OF ICE SYSTEM



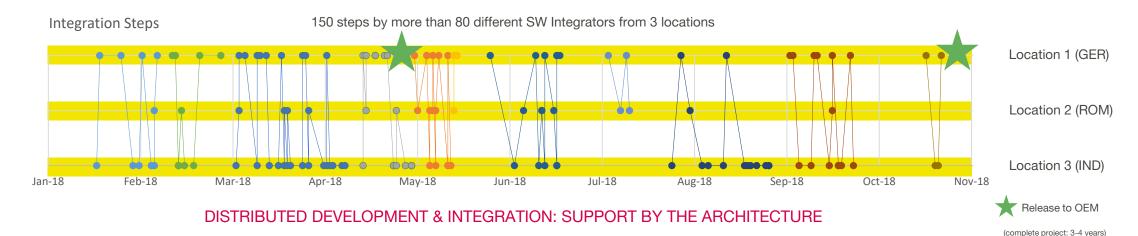
MORE SW NEEDED TO REDUCE FUEL CONSUMPTION !

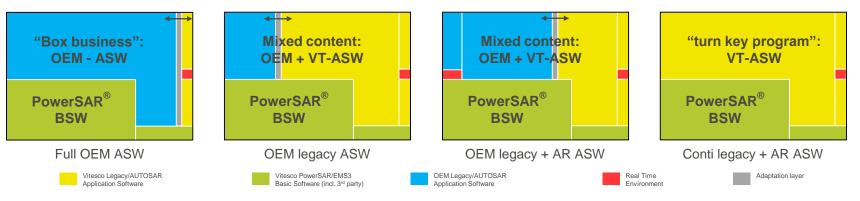


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AFFORDABLE SOLUTIONS

REUSE TO SHORTEN DEVELOPMENT CYCLES, REDUCE DEVELOPMENT COSTS





OEM DEVELOPS HIS PART INDEPENDENTLY AND INTEGRATES / BUILDS AGAIN THE SW

HIGHER INTEGRATION BETWEEN PARTNERS



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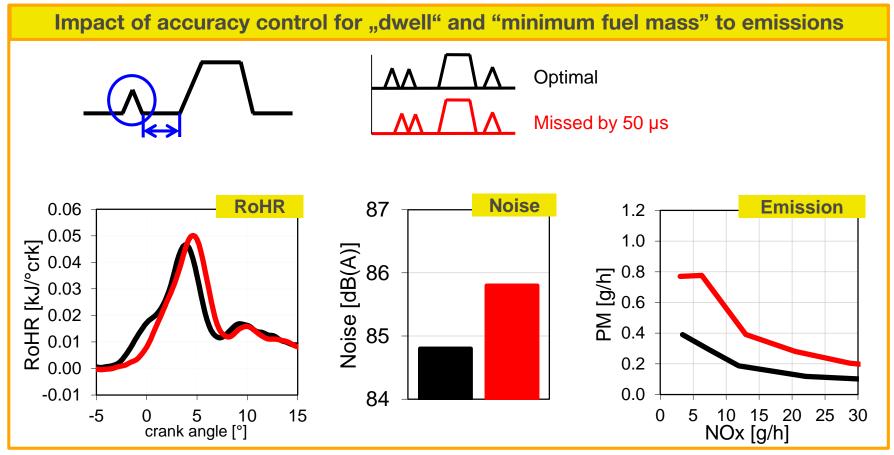
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REAL TIME SW

THE RIGHT VALUE AT THE RIGHT TIME



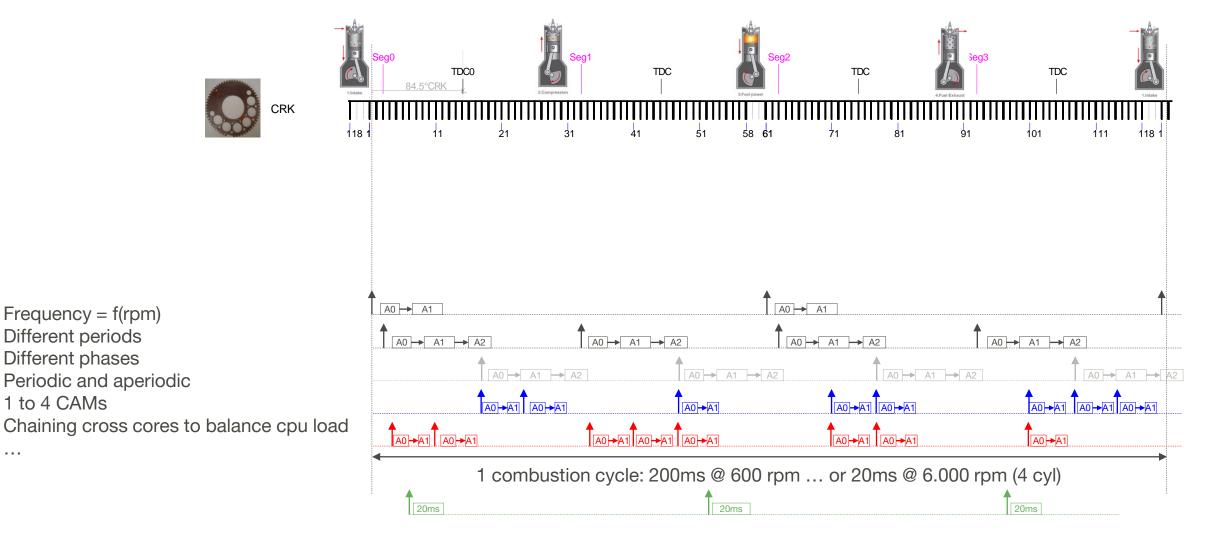
at n= 1500 min⁻¹, p_{mi}= 4,2 bar, HR50= 8°KW, EGR=35%

THE RIGHT TIMING IS IMPORTANT !



ANGULAR TIME

SW DYNAMICS DRIVEN BY ACTUATOR CONTROL DYNAMICS



ANGULAR TASKS AND TIME BASED TASKS RUNNING ON THE SAME CPU



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1.

2.

3.

4

5.

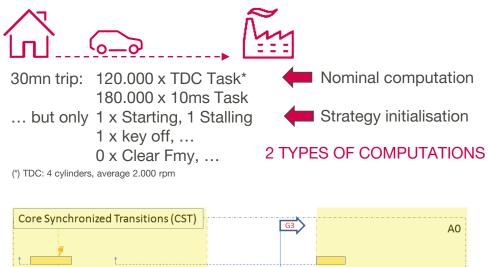
6.

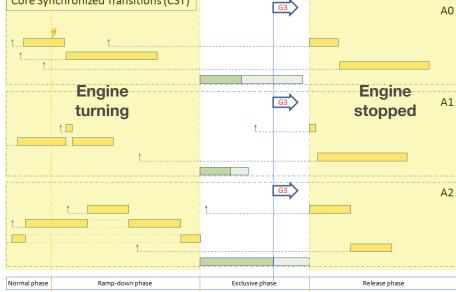
7.

. . .

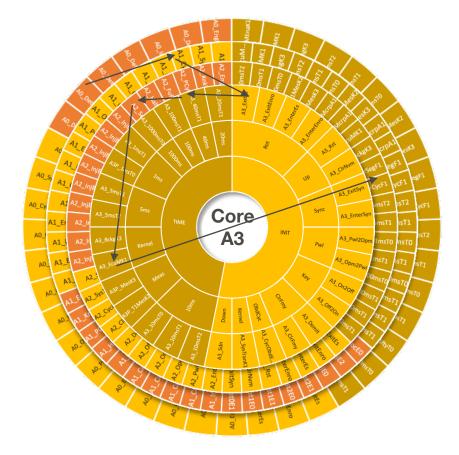
SPORADIC TIME

NEED OF COHERENT SYSTEM STATE CROSS ALL TASKS ON ALL CORES





SYSTEM TRANSITION IN A PROTECTED MODE



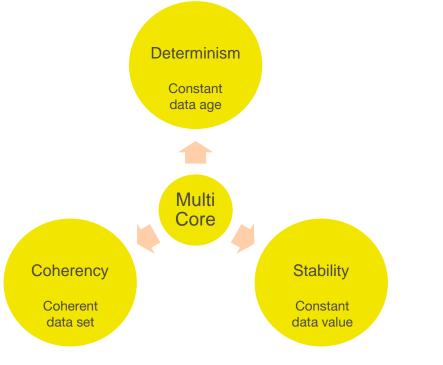
BALANCE BETWEEN 3 "TIME DOMAINS" ... ON ALL CORES

DATA COMMUNICATION BETWEEN TASKS & DOMAINS TO BE CONTROLLED

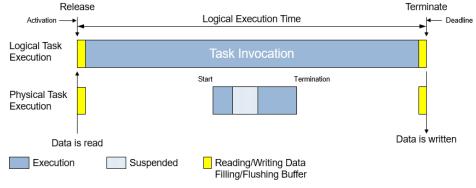


INTER-TASK COMMUNICATION

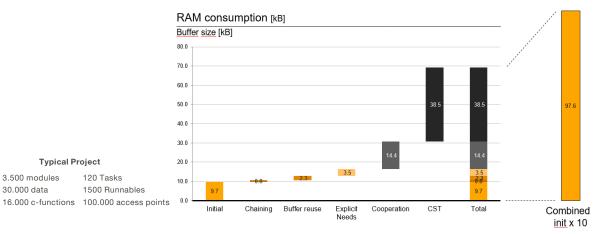
DIFFERENT TYPES OF INTEGRITY



3 TYPES OF INTEGRITY



LOGICAL EXECUTION TIME TO ENSURE DETERMINISM



CRITICAL: EFFICIENCY OF BUFFERING ALGORITHM

INEFFICIENT STRATEGY MAY LEAD TO ... NON-DISTRIBUTABLE SW



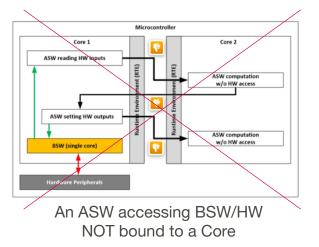
CORE ABSTRACTION FOR EASIER SW DISTRIBUTION

3 LEVELS OF ABSTRACTION

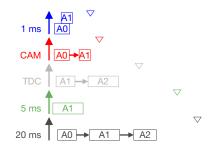
PROBLEM: CORE ALLOCATION IS A MULTI-CRITERIA CHOICE

Event availability	Link to Safety Core / Active Lockstep
 A function has a required Rate: 1st criteria for integration 	 Safety relevant functions have to be processed on Core with Active Lockstep
Core affinity	OEM/Other parties constraints
 > Vs. HW feature (e.g. dbl fpu,) , other function > OEM-SW fix some distribution 	
→ Limit risk for data written at different ratε	Order of Runnables matters !
Last Writer Wins (Lww) situations	Sequencing constraint
 Some functions are risky to distribute (complex real time, not multi-core ready) 	 Higher freedom for introduction of more functions in a late step
Distributivity of the function	CPU load balancing

BSW SERVICES AVAILABLE ON EACH CORE

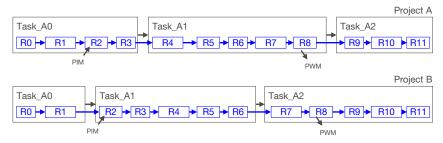


SW ARCHITECTURE INDEPENDENT OF HW FEATURES



Standard task setup for all projects despite different HW configurations (µC)

ASW INTEGRATION INDEPENDENT OF ABSTRACT CORE



CORE ABSTRACTION FOR HIGHER SYNERGY BETWEEN PROJECTS, EASIER INTEGRATION

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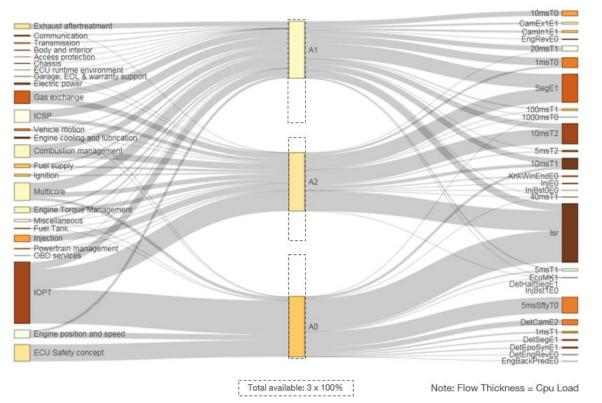
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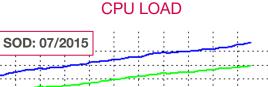


CORE DISTRIBUTION

ENSURING SYSTEM HEALTH DESPITE FUNCTIONAL CONTENT INCREASE







60

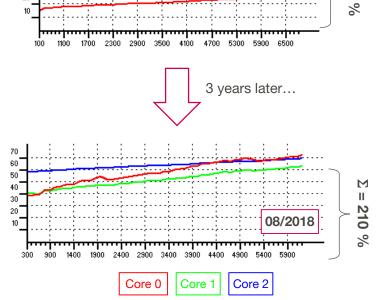
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LOAD BALANCING PREPARES THE SYSTEM FOR FUTURE EVOLUTIONS

(EVENT) RESPONSE TIME MONITORING IS A BETTER INDICATOR OF THE SYSTEM HEALTH



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THANK YOU FOR YOUR ATTENTION