Modélisation UML/MARTE de SoC et analyse Temporelle basée sur l’approche synchrone

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Introduction

High level design specification

Synchronous clock analysis for efficient system redesign

Concluding remarks
Increasing dramatically in our day-to-day life

Chips growing in size and speed, Driving up to a computational complexity

- Shorten design cost and time-to-market
- Guarantee QoS constraints and efficient resource distribution

- System design at a high-level abstraction : UML/ MARTE (Modeling and Analysis of Real Time Embedded systems) and the synchronous approach
Gaspard framework

Oriented towards the Co-design of parallel software and hardware: http://www2.lifl.fr/west/gaspard/index.html
Overall approach

Logical clock extraction

Application

Association

Clock mapping synthesis

Deployment

Physical clock extraction

Architecture

Physical IPs refactoring
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Application specification

- Specification of functional aspects

- Logical clock insertion using CCSL of MARTE
Repetitive Structure Modeling (RSM)

- Task expressing how a single subtask is repeated
- Building patterns from arrays
- Instances operates on subarrays or patterns with the same shape
Architecture specification

- A multiprocessor architecture structure
Architecture specification (cont’d)

- IP deployment for processor **Proc1**

- Physical clock synthesis
  - **Proc1** = 15 MHz, **Proc3** = 30 MHz
Association specification

- Association of application and architecture
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Clock Merging

- Clock Merging

- QoS constraint violated

- Incoherence between designer constraints and resources capacity
Solution 1: Delaying the processors activation

- Delaying the activation of **Proc3** (Cohen et al., 2006)

  ![Clock Cycle Diagram]

  - Advantage: QoS constraint Verified
  - Inconvenient: Temporary memory needed to buffer unconsumed data
Solution 2: Physical IPs modification

- Modification of physical clocks
  - **Proc1** = 30 MHz, **Proc3** = 15 MHz

- Clock merging

| IdealPhysicalClk | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ClkProc1         | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ClkProc3         | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |

- Advantage: QoS requirements Verified

- Inconvenient: Temporary memory needed to buffer unconsumed data
Solution 2: Physical IPs modification (cont’d)

- Modification of physical clocks
  - \( \text{Proc1} = 90 \text{ MHz}, \text{Proc3} = 90 \text{ MHz} \)

- Advantages
  - QoS requirements Verified
  - No buffering system needed since producers and consumers are synchronized
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- System specification using UML/MARTE and synchronous approach: system structure modeling and clock specification

- Clock analysis for QoS constraint verification and efficient system redesign, based on the synchronous approach

- Benefits: Efficient frequency and memory distribution