Cache-aware Schedulability Analysis of PREM Compliant Tasks

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Real-Time & Embedded Computing Systems

Presentation Contents

01
Introduction and Motivation

PREM Model, and
Problem definition

02
Cache-aware PREM Model

DRCB-only Approach
FDCB-DRCB Approach

03
Experimental Setup and Results

Experiments performed under different settings and parameter values

04
Conclusions and Future works

Conclusions and potential future research directions

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Contention due to shared resources, e.g., main memory, between tasks can have a significant impact on WCET/WCRT of tasks

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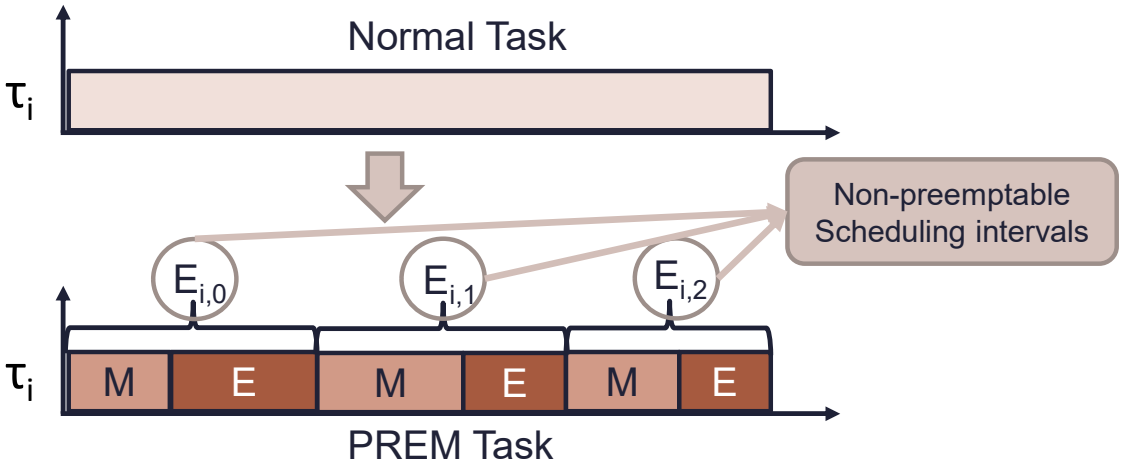

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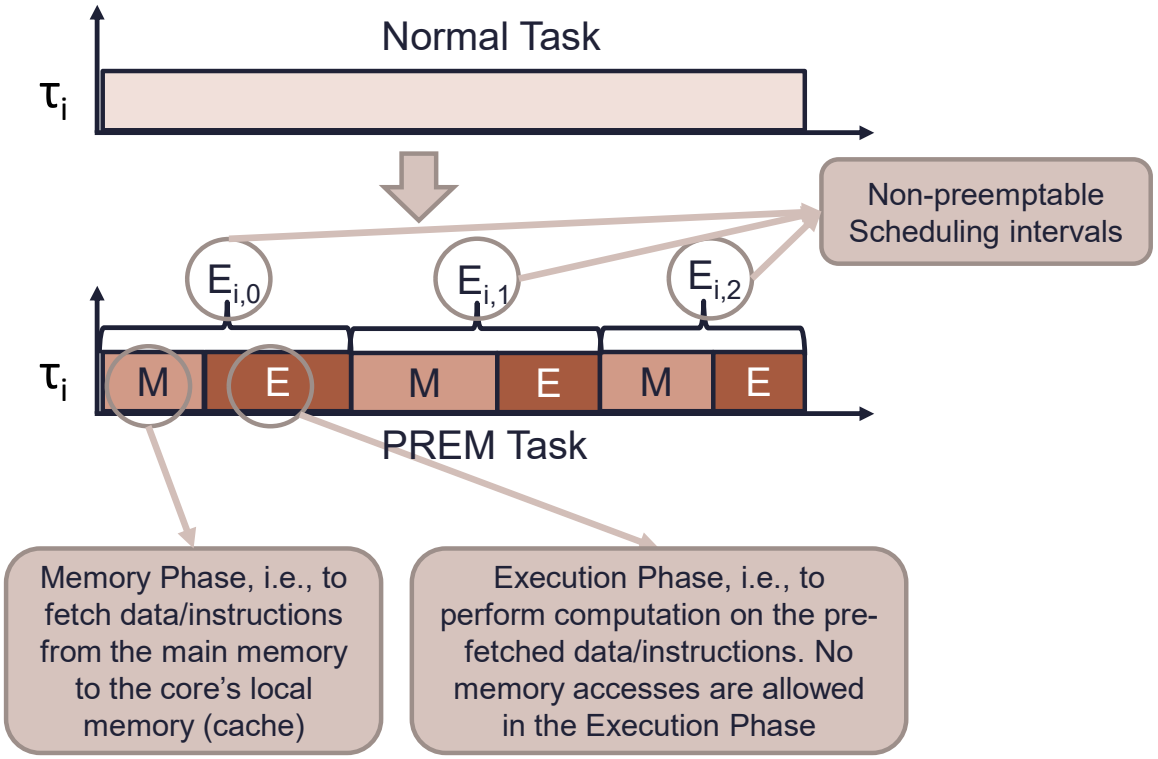

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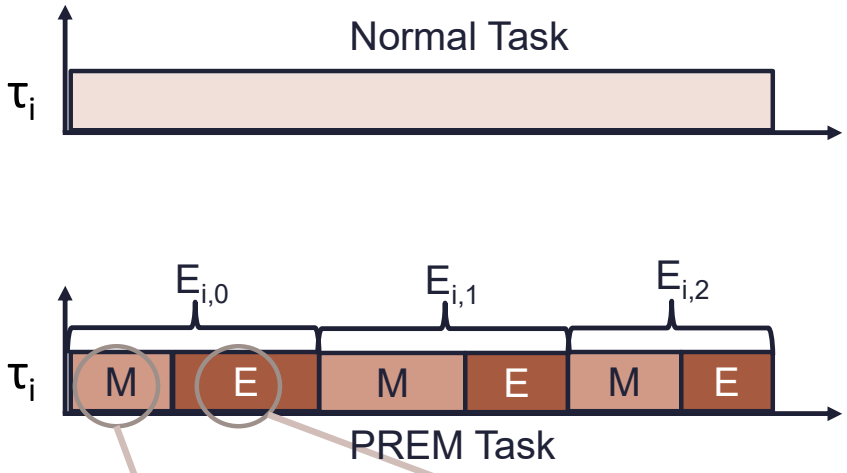

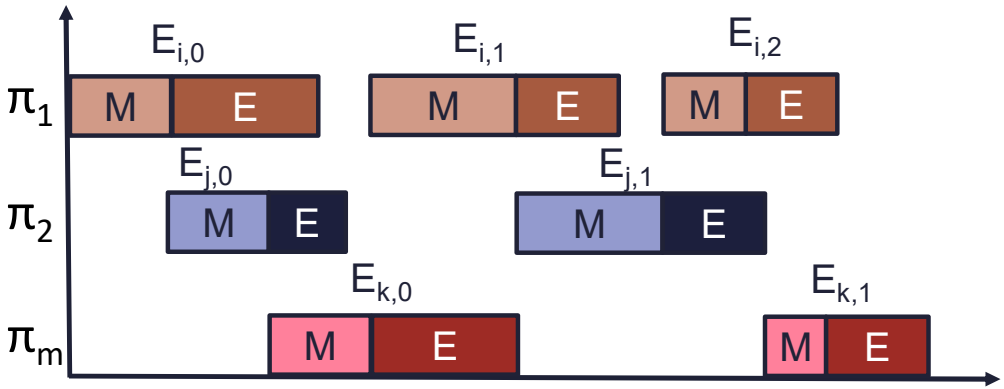

Memory Phase, i.e., to fetch data/instructions from the main memory to the core's local memory (cache)

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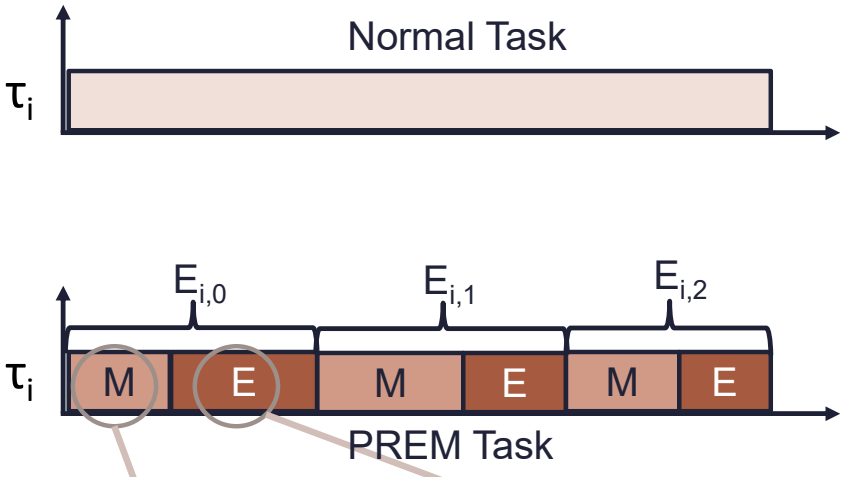

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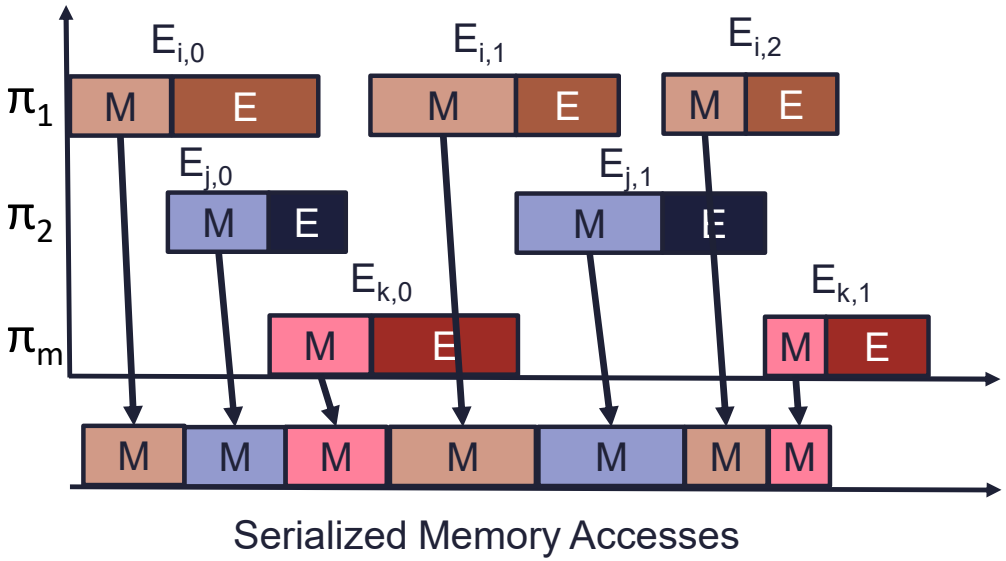

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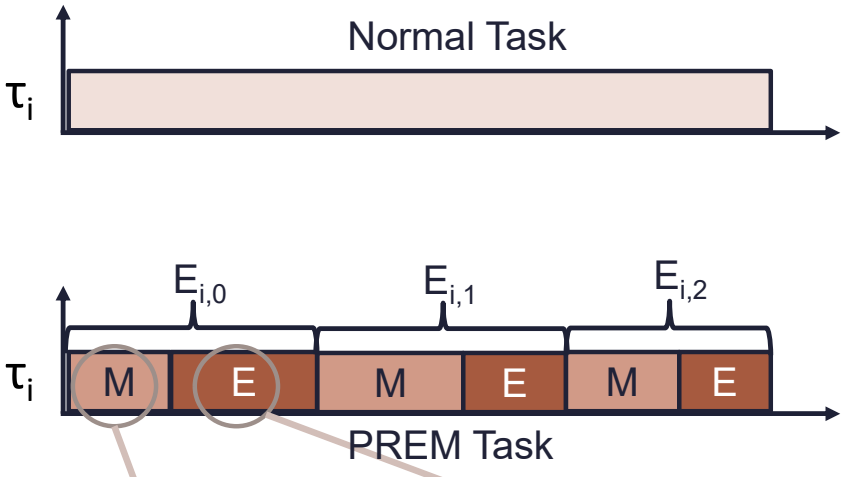

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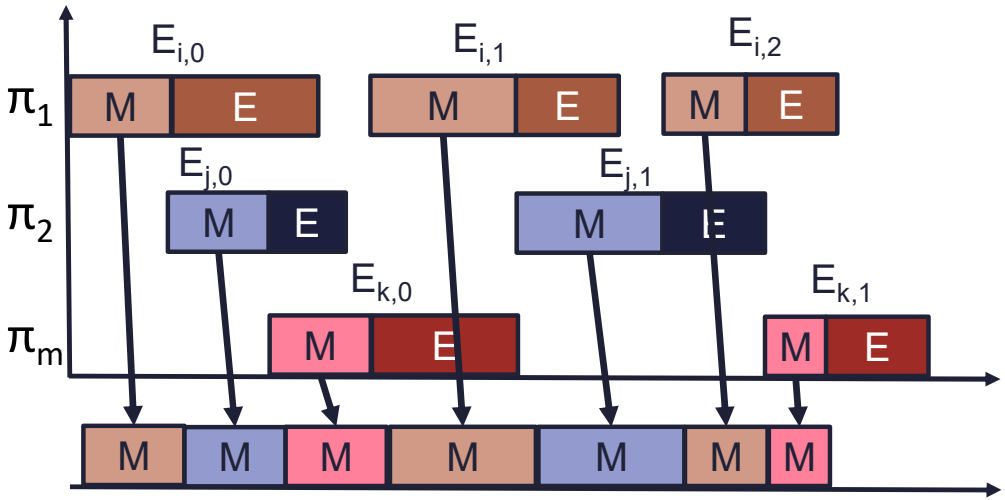

Serialized Memory Accesses

PREM can significantly reduce/eliminate contention due to shared main memory

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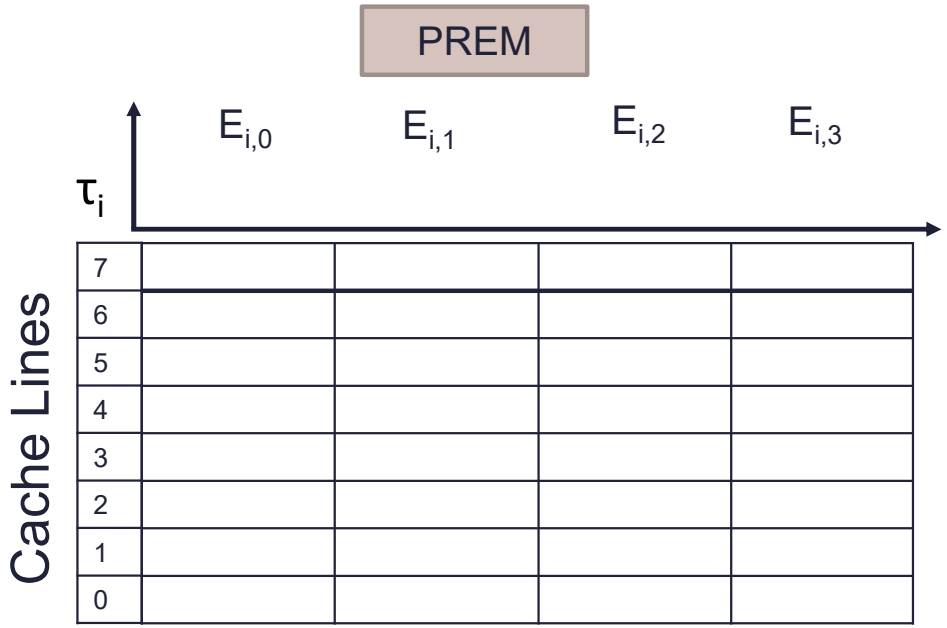

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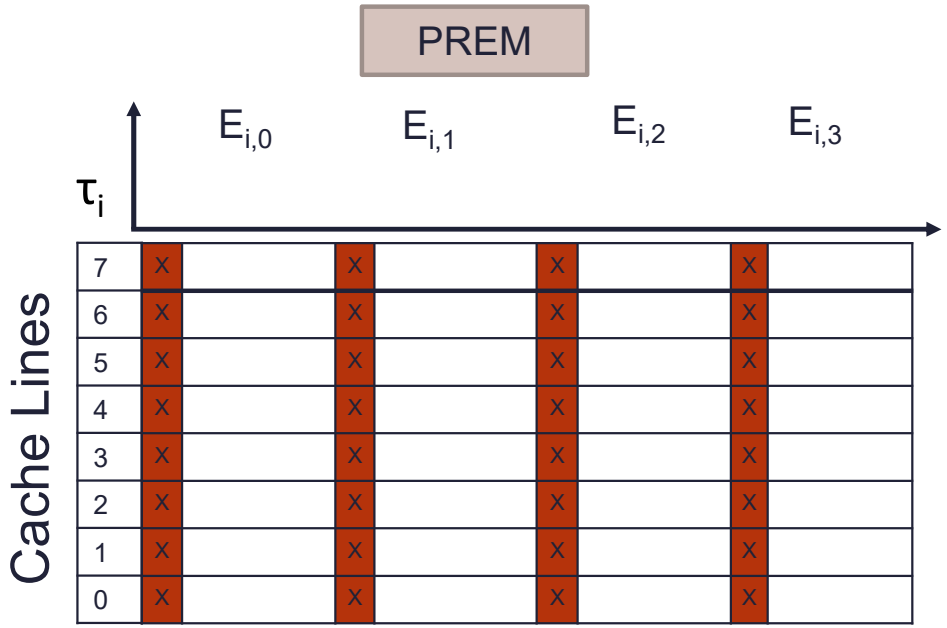

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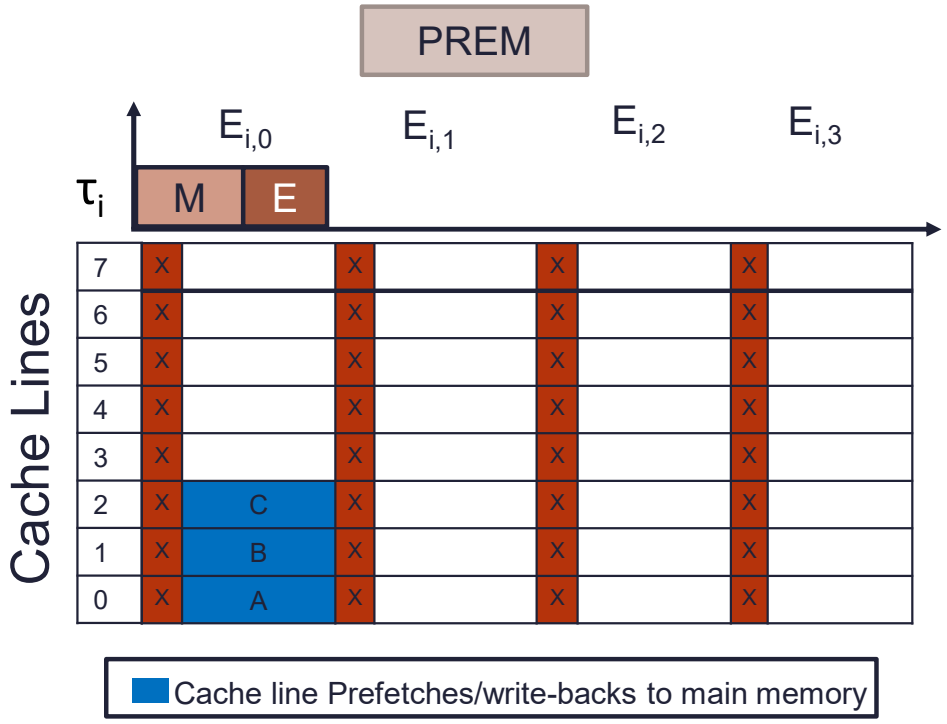

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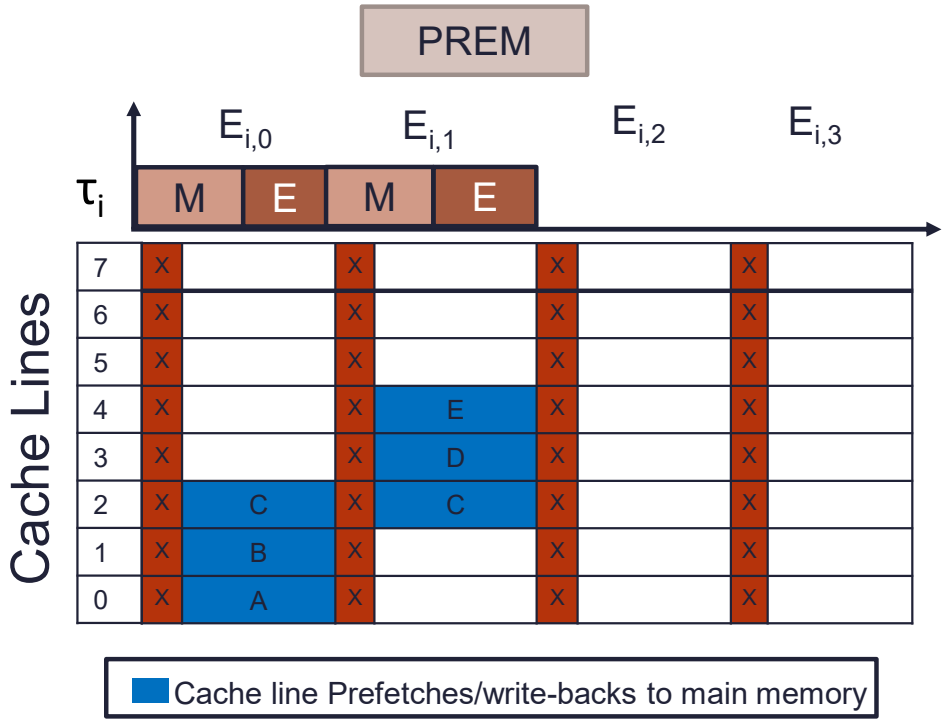

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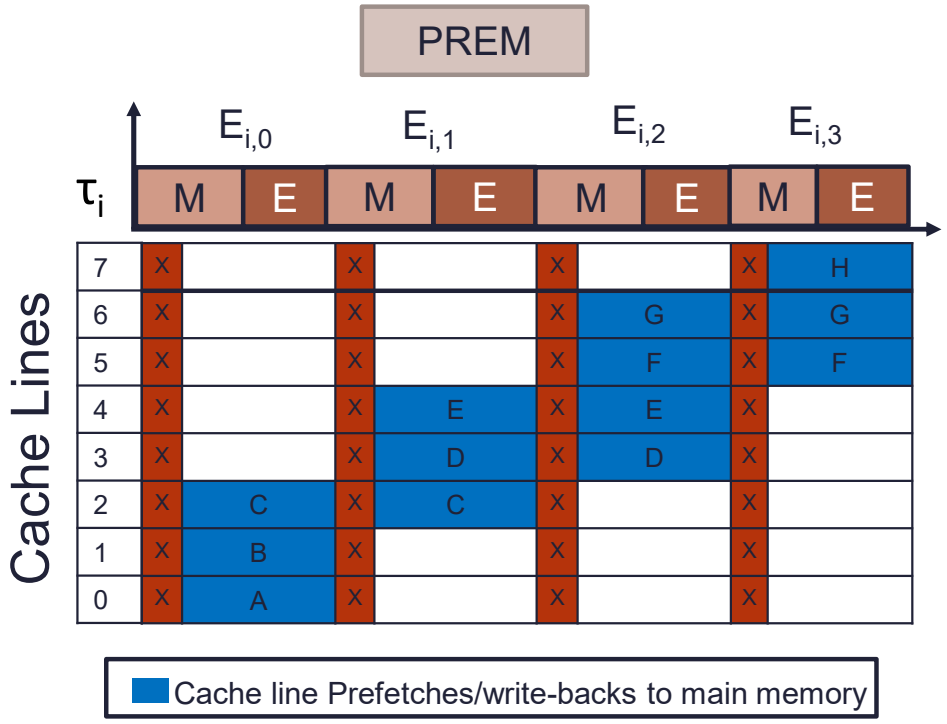

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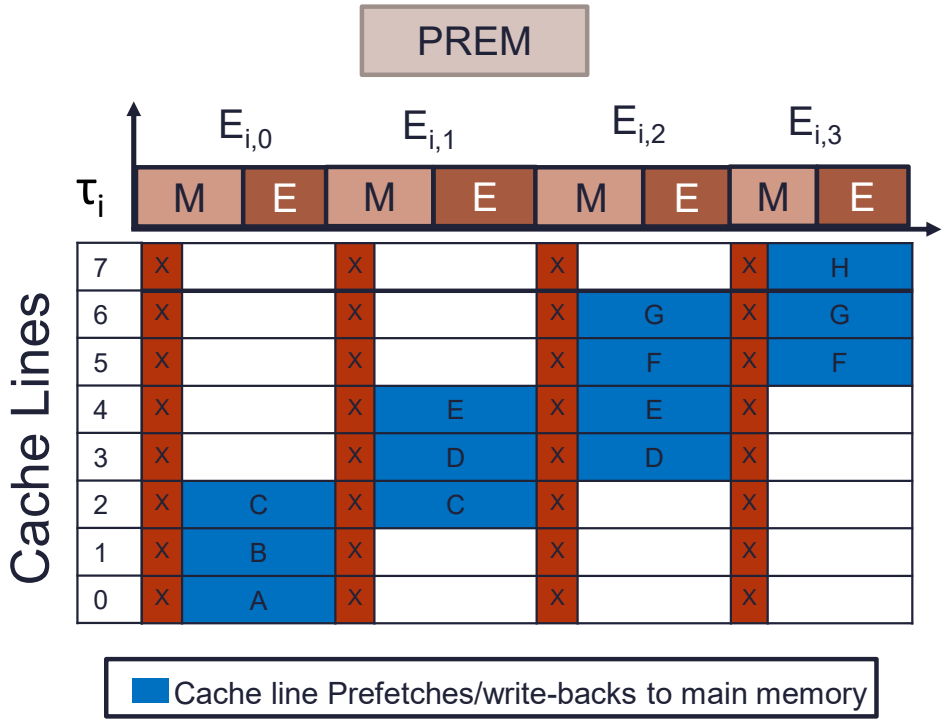

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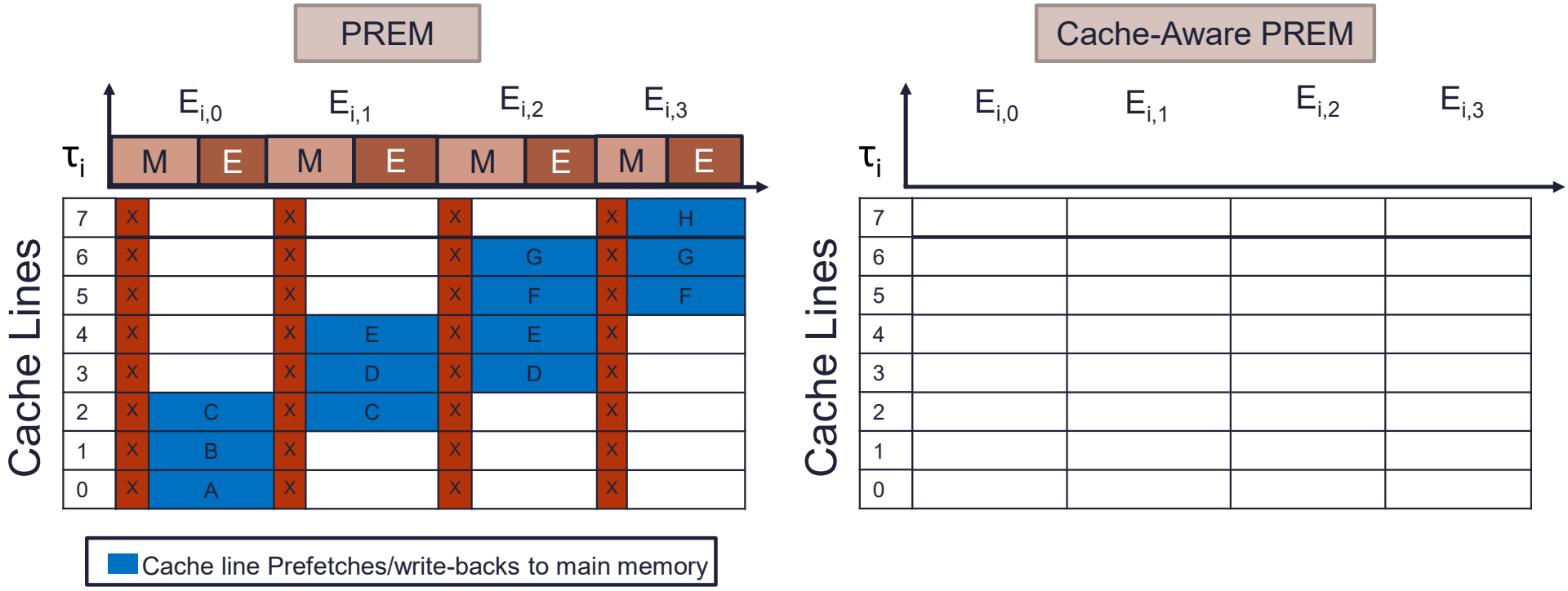

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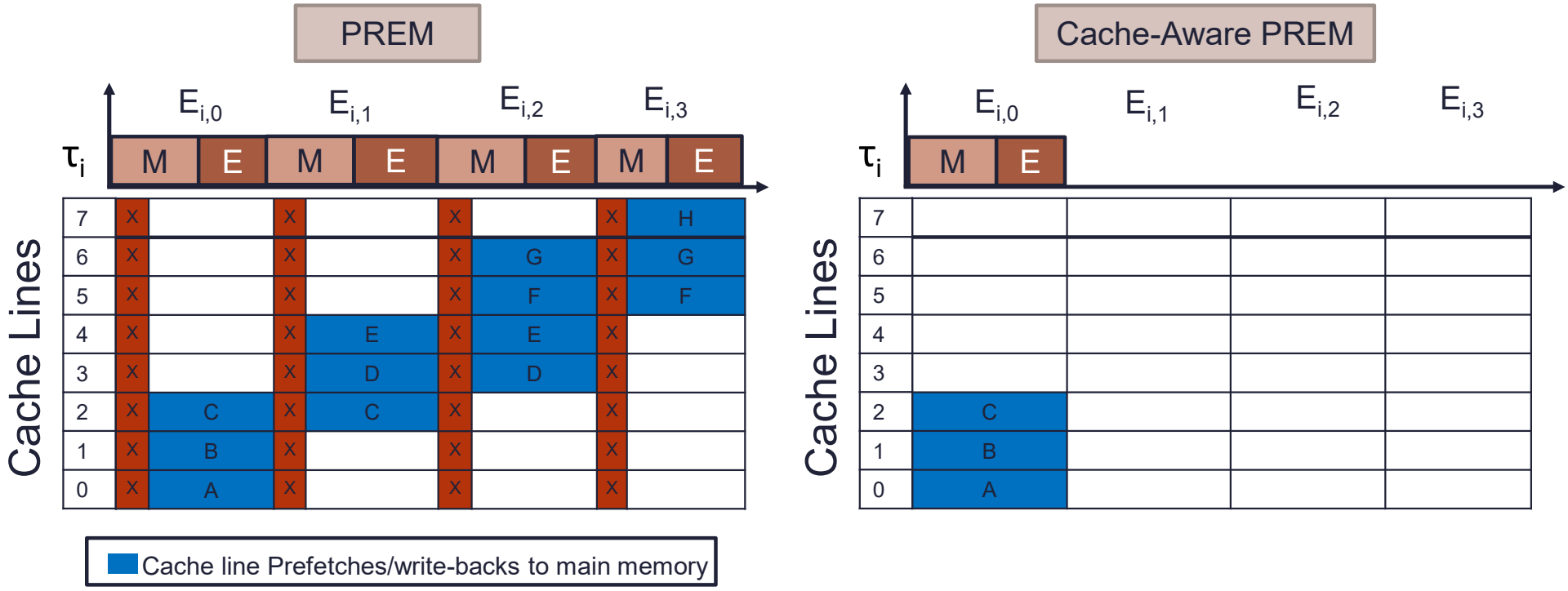

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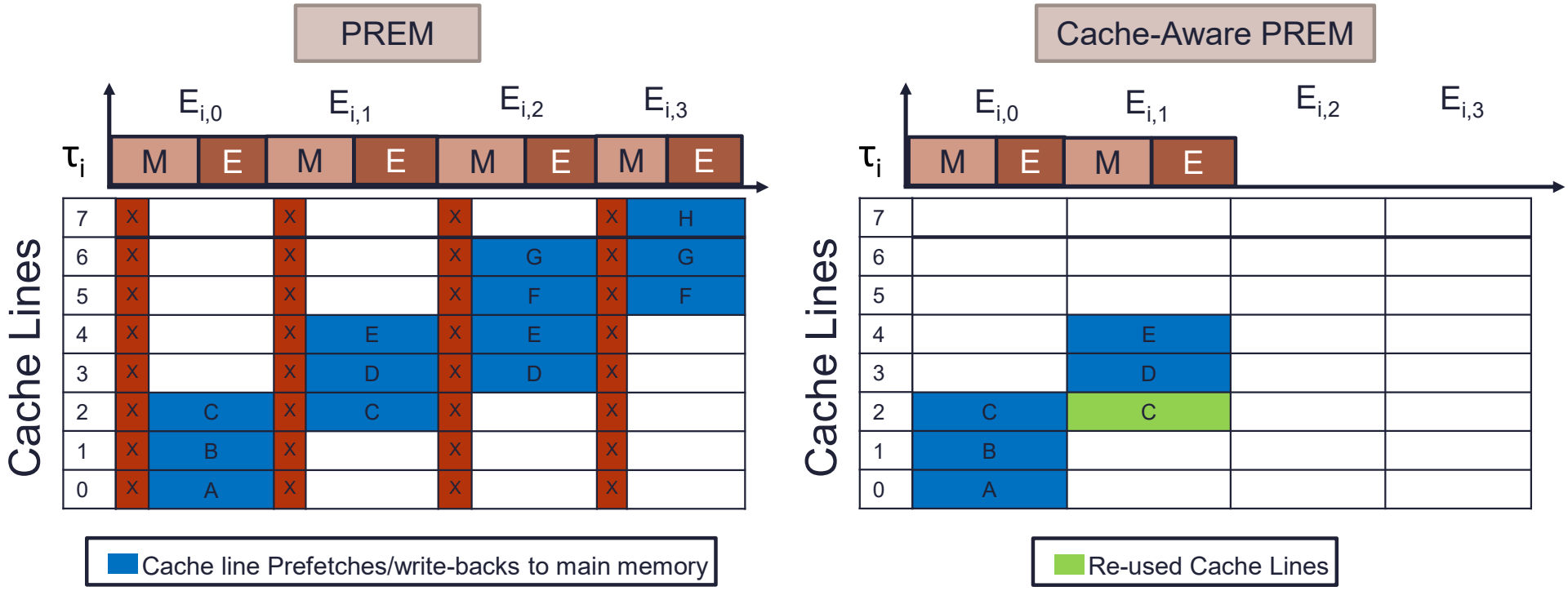

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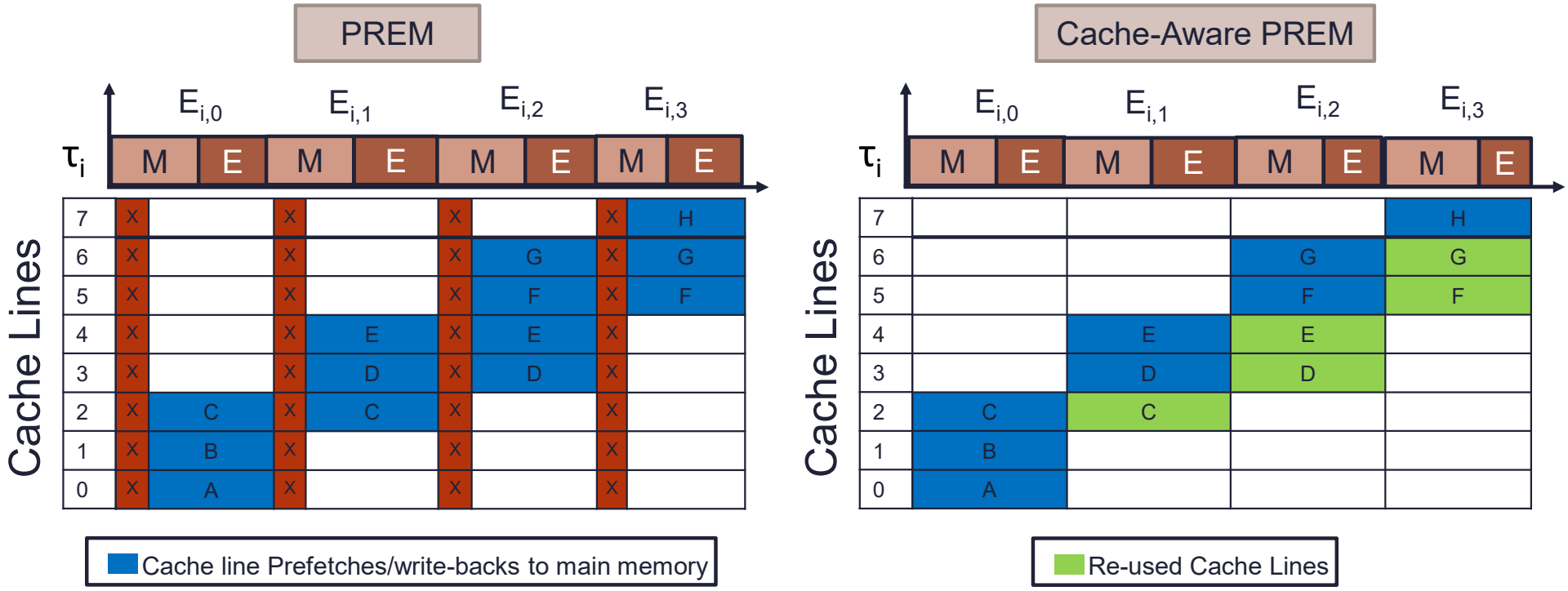

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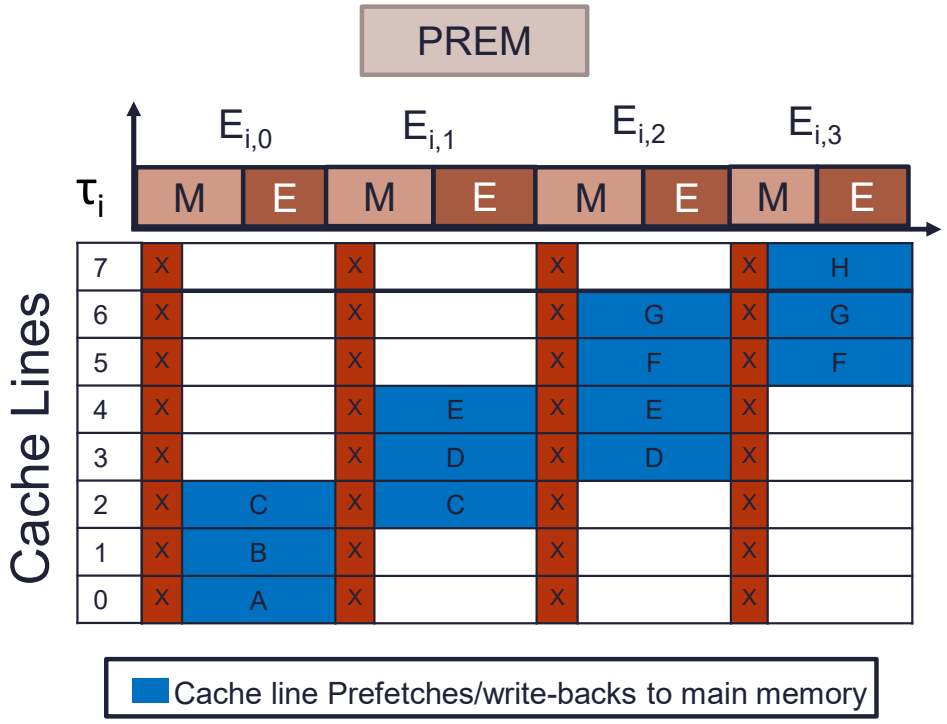

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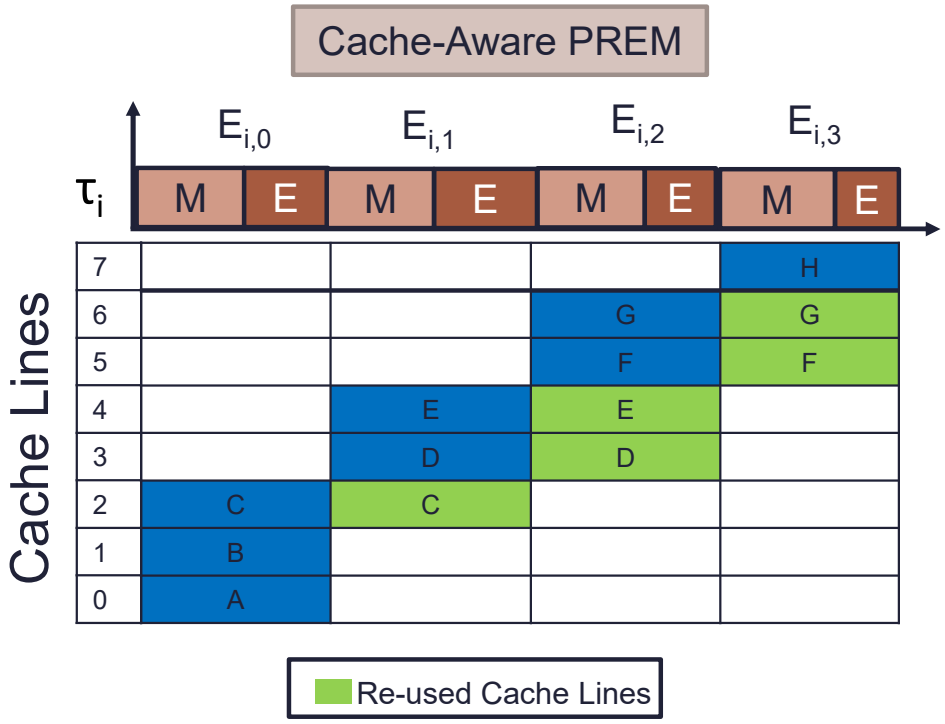

Total Memory Accesses = Total Prefetches + Total Write-backs
= 8 + 8 = 16

Contribution: Cache-aware schedulability analysis of PREM tasks

- Preciser estimate of cache line prefetches -> DRCB-only Approach
- Tighter bound on cache line write-backs -> FDCB-DRCB Approach

Cache-Aware PREM: DRCB-only Approach

- What are Definitely Reused Cache Blocks (DRCBs)?

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  Memory blocks that are cached at the end point E of a scheduling interval E_{i,j-1} and are reused at some program point F in scheduling interval E_{i,j}, without being evicted on any possible execution path between E to F.

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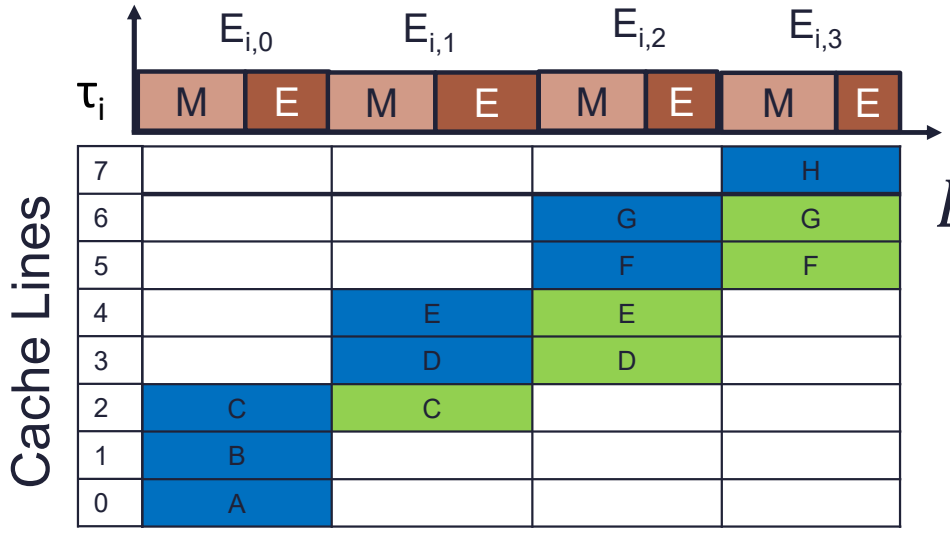

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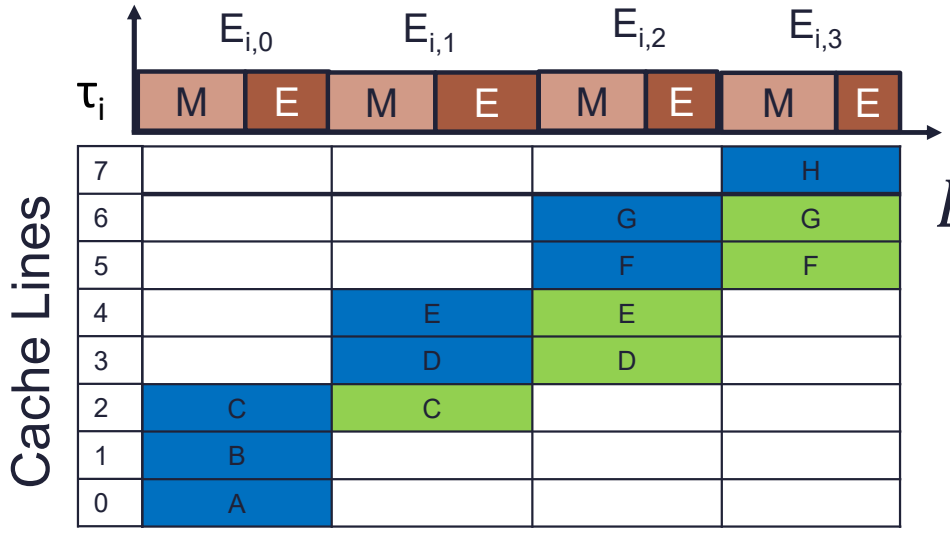

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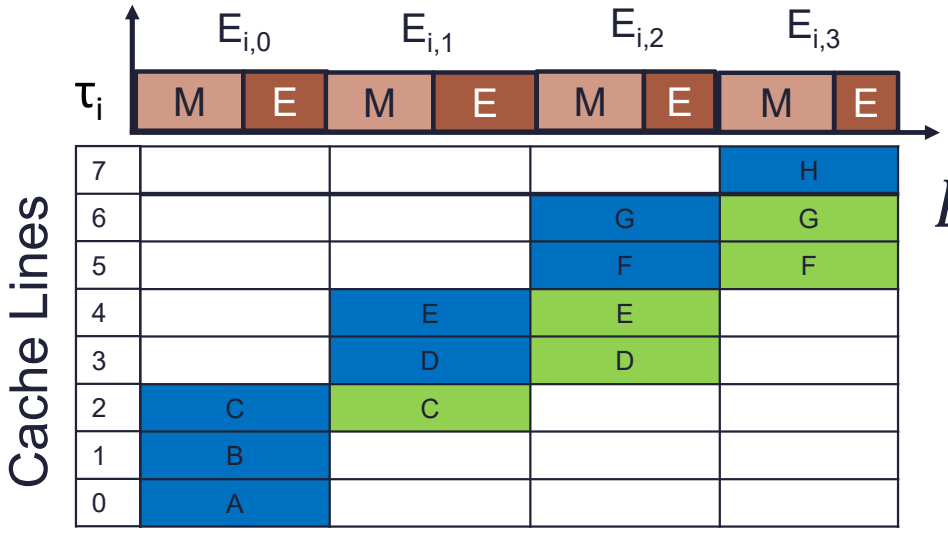

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$$DRCB_i = \{C, D, E, F, G\}$$

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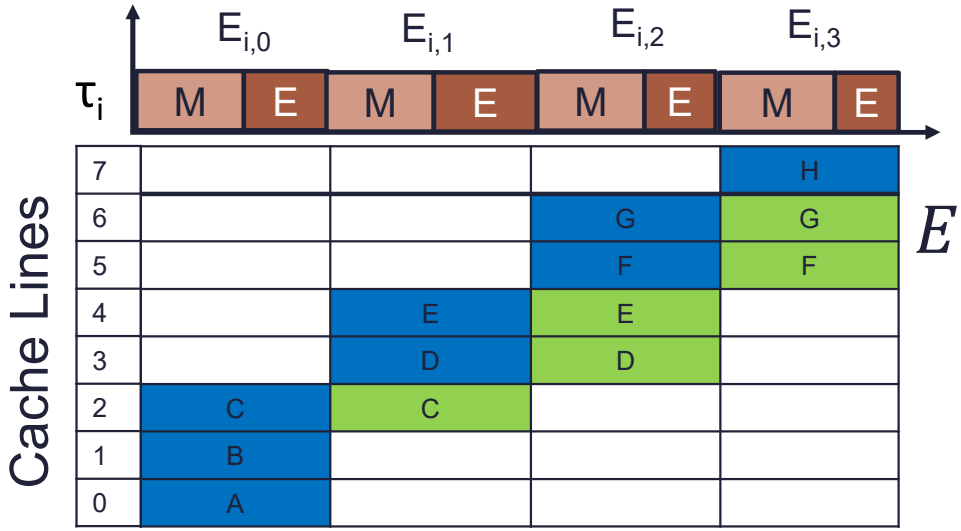

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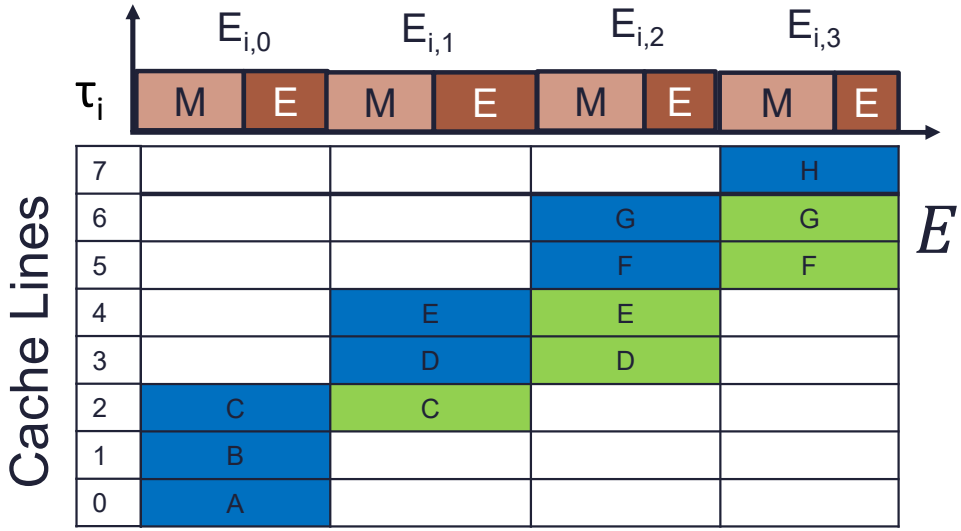

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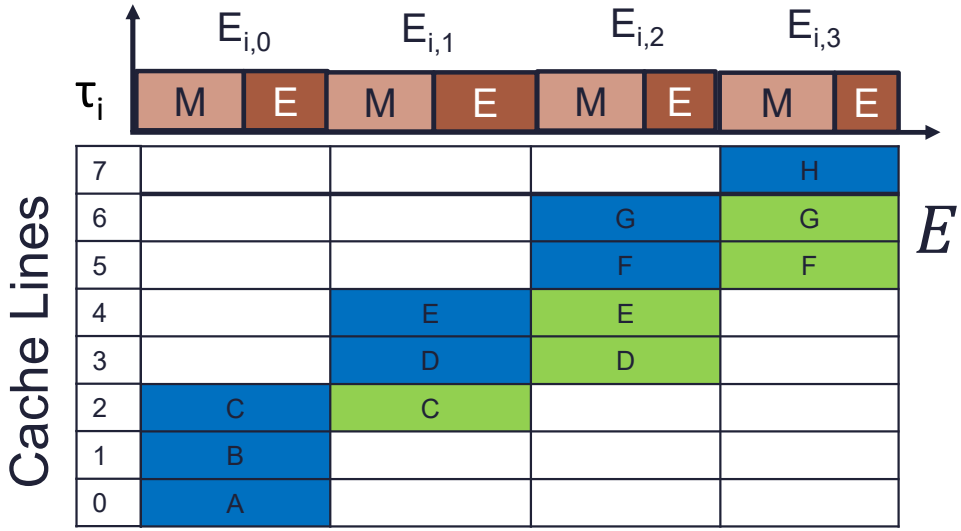

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  A scheduling interval E_{i,j} only needs to prefetch ECBs that are not its DRCBs

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$$Memory\ blocks\ prefeteched\ by\ E_{i,j} = ECB_{i,j}/DRCB_{i,j}$$

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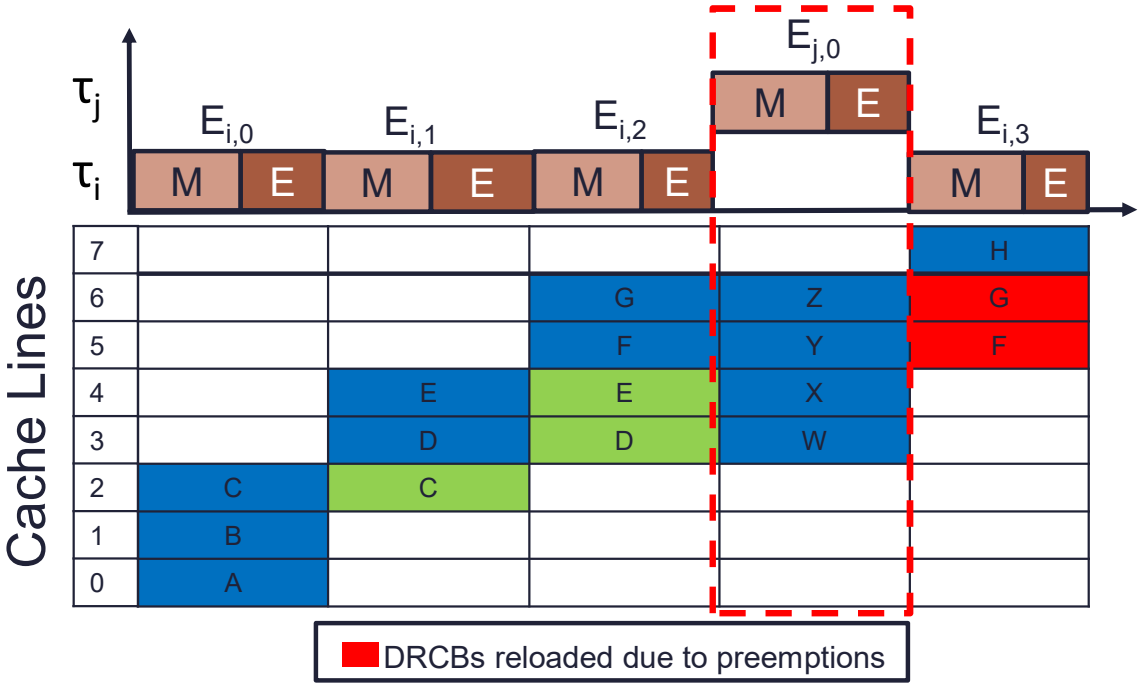

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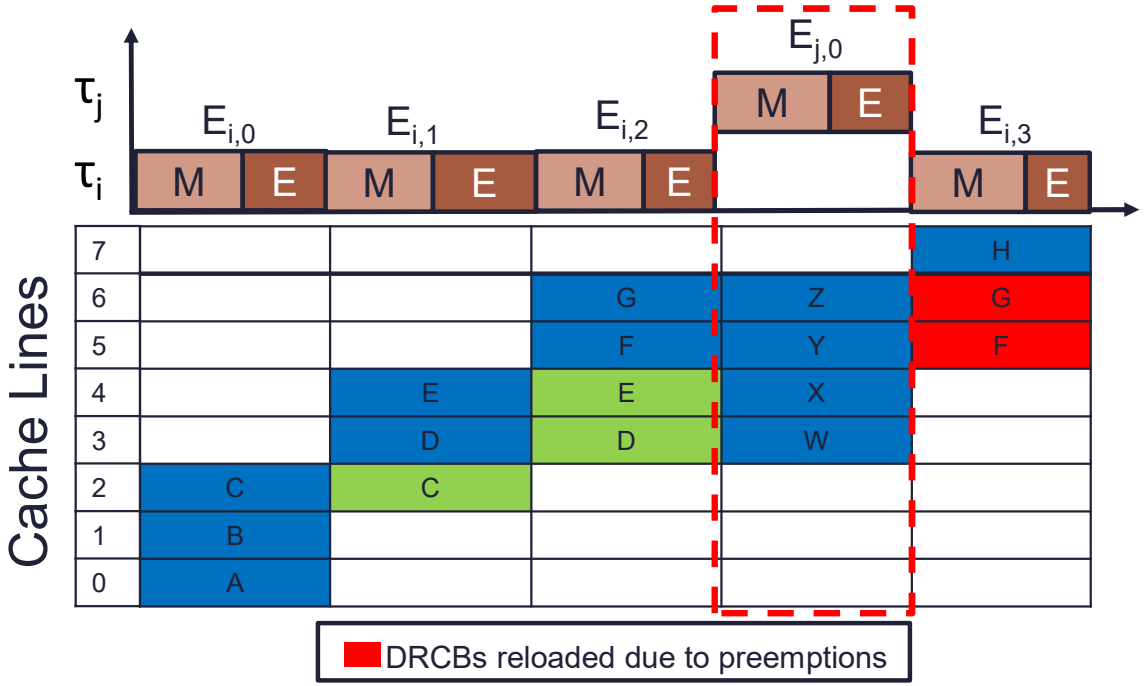

$$\underbrace{DRCB^{E}_{i,j}}_{\text{DRCB of E\_\{i,j\} evicted due to preemptions}} = DRCB_{i,j} \bigcap \{ \bigcup_{\forall k \in hp(i)} ECB_k \}$$

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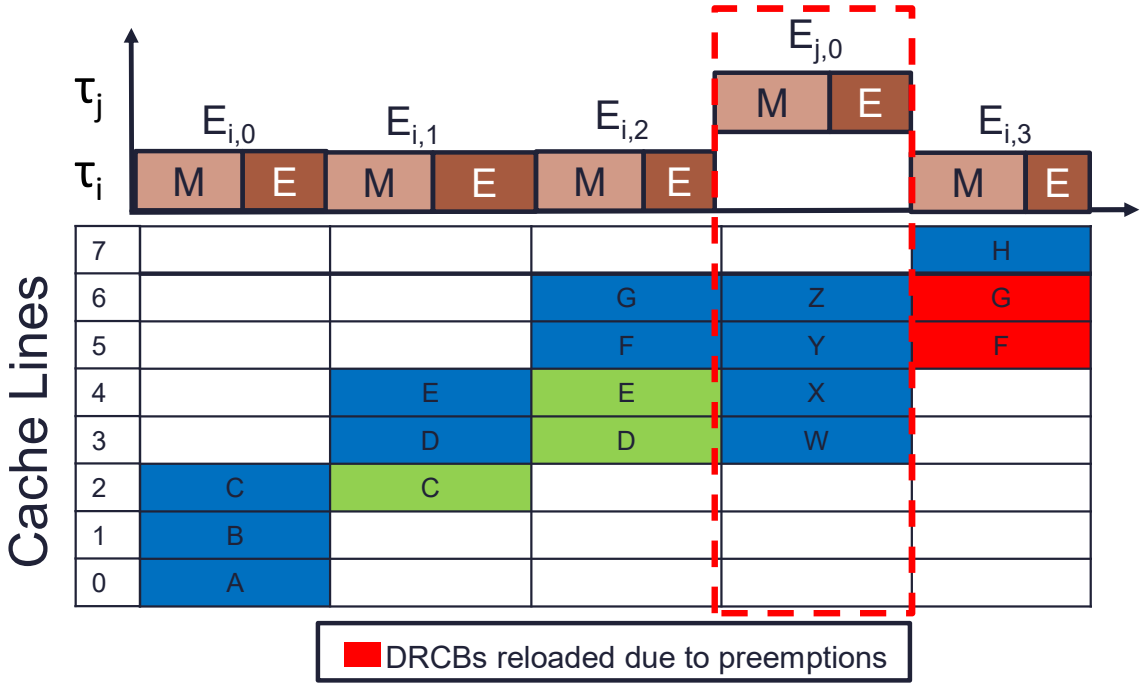

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$$\underbrace{ECB^{P}_{i,j}}_{\text{Prefetches during } E_{i,j} \text{ with cache reuse}} = \{ ECB_{i,j} \setminus DRCB_{i,j} \} \bigcup DRCB^{E}_{i,j}$$

$$\left| ECB^{P}_{i,j} \right| \leq |ECB_{i,j}|$$

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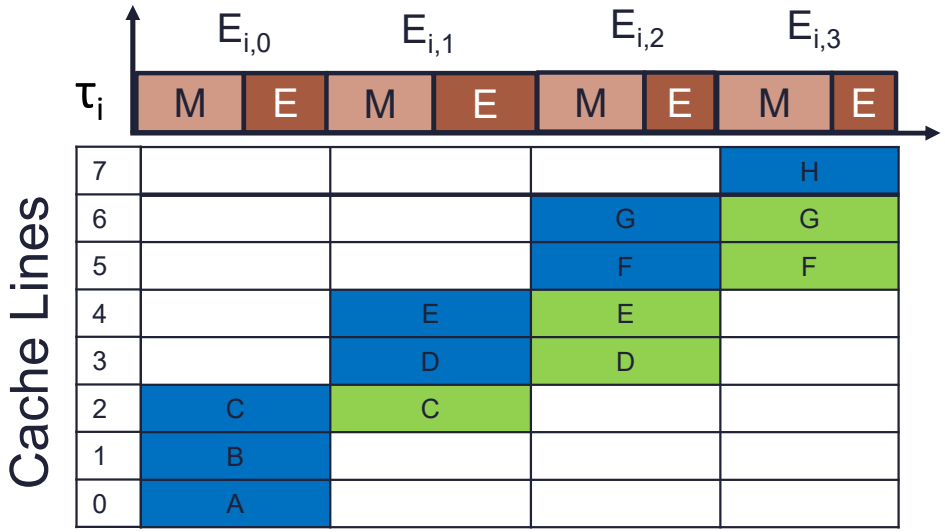

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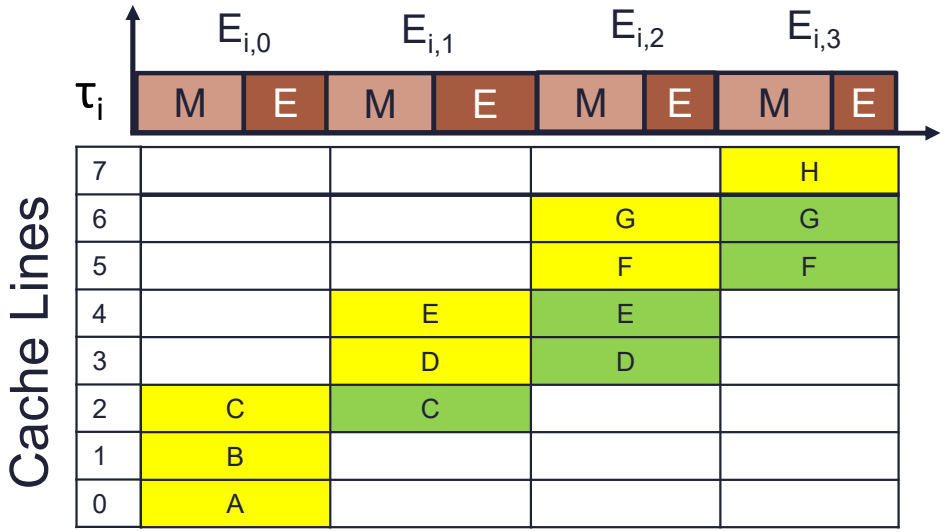

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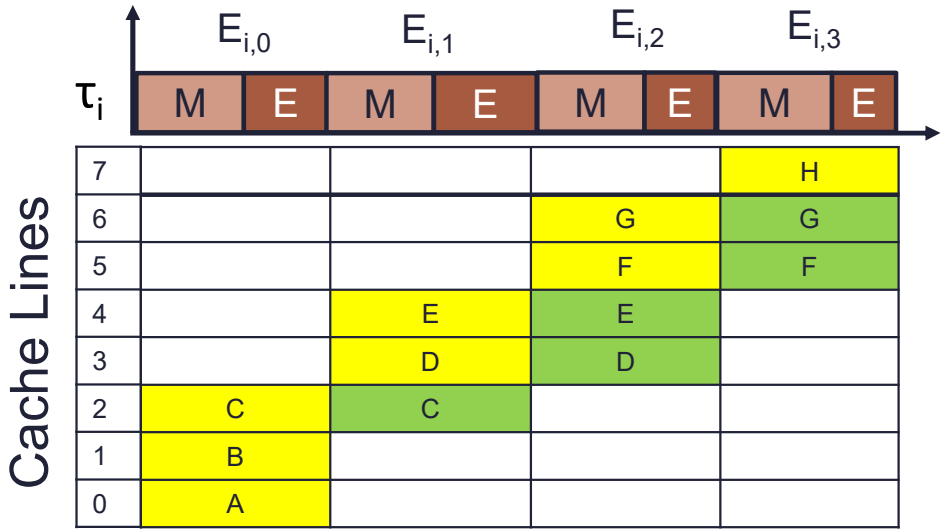

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Actual number of write-backs depend on the number of dirty cache lines

Cache-Aware PREM: FDCB-DRCB Approach

- What are Final Dirty Cache Blocks (FDCBs)?

  Memory blocks that may be written to during the execution of a task/scheduling interval and may still be available in cache after the completion of that task/scheduling interval.

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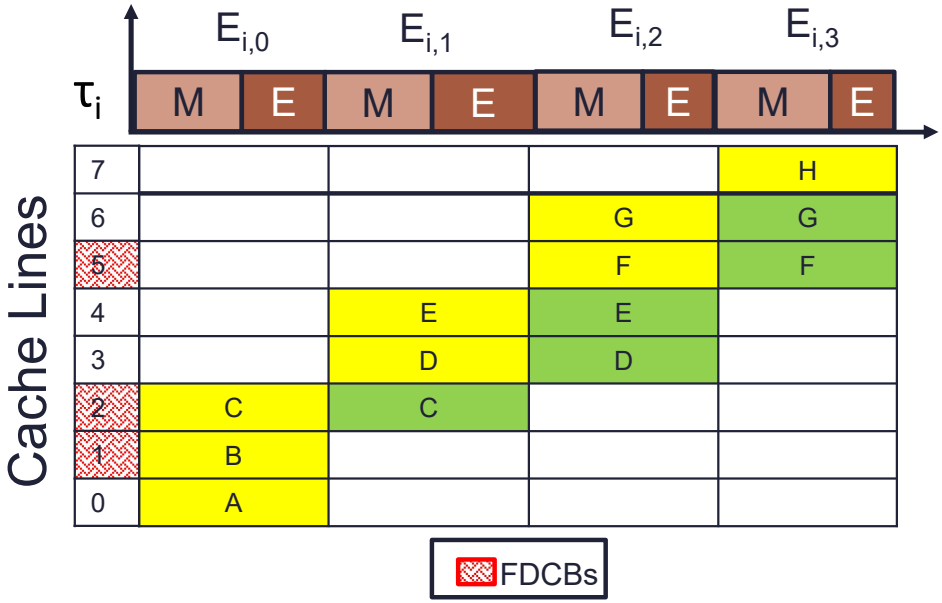

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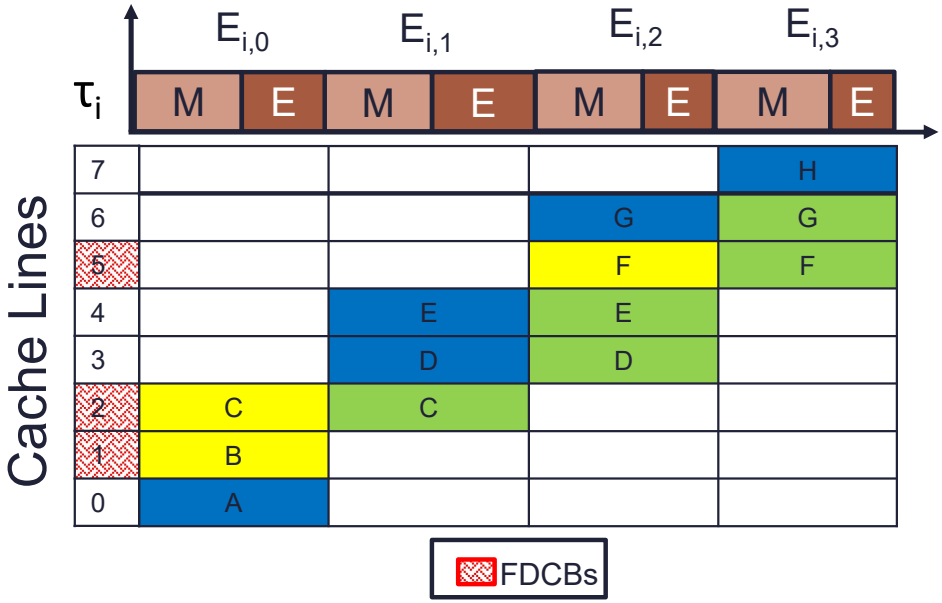

$$WB_{i,0} = \{A, B\}, WB_{i,1} = \{\}$$

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Cache-Aware PREM: FDCB-DRCB Approach

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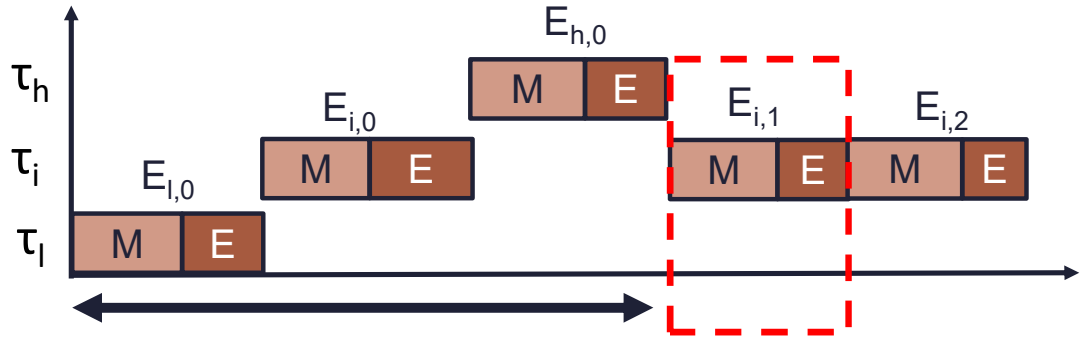

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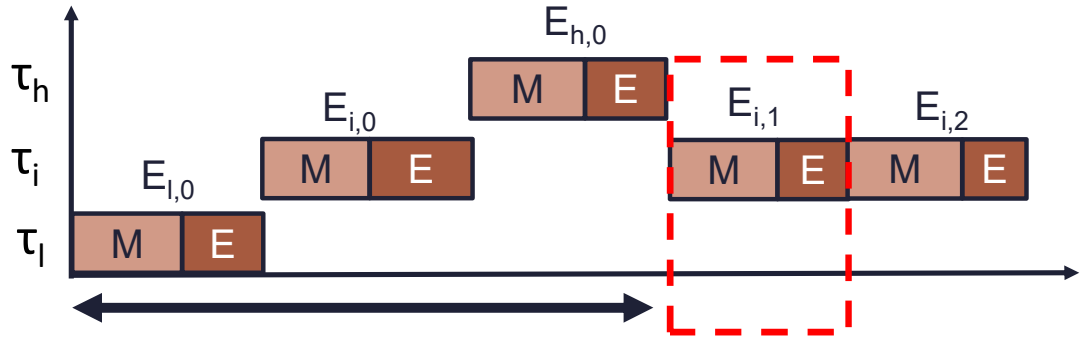

$$\underbrace{WB_{i,j}^{lp}}_{\text{Write-backs due to tasks in lp(i)}} = \left(\bigcup_{\forall l \in \mathrm{lp}(i)} FDCB_l \setminus \bigcup_{\forall k<j} ECB_{i,k} \right) \bigcap ECB_{i,j}$$

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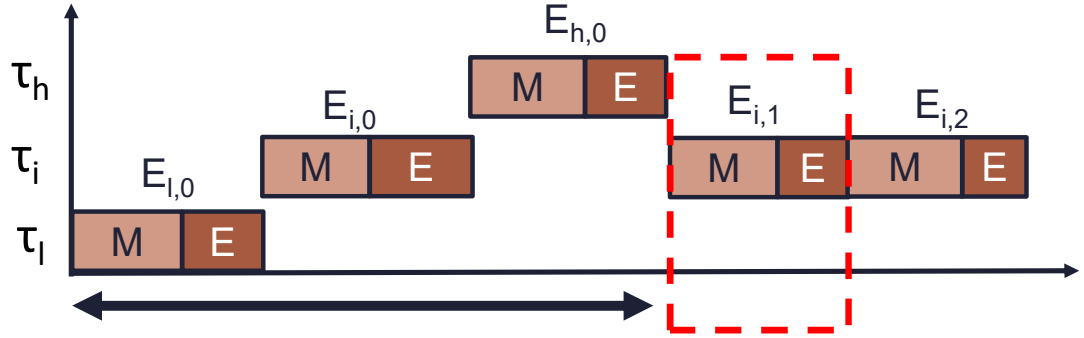


$$\underbrace{WB^{lp}_{i,j}} = \left(\bigcup_{\forall l \in \mathrm{lp}(i)} FDCB_l \setminus \bigcup_{\forall k<j} ECB_{i,k} \right) \bigcap ECB_{i,j} \qquad \underbrace{WB^{hep}_{i,j}} = \left(\left(\bigcup_{\forall h \in hep(i)} FDCB_h \right) \bigcap ECB^R_{i,j} \right) \bigcup DRCB^E_{i,j}$$

Write-backs due to tasks in lp(i)

Write-backs due to tasks in hep(i)

$$WB^{tot}_{i,j} = WB^{lp}_{i,j} \bigcup WB^{hep}_{i,j}$$

Cache-Aware PREM: WCRT Analysis

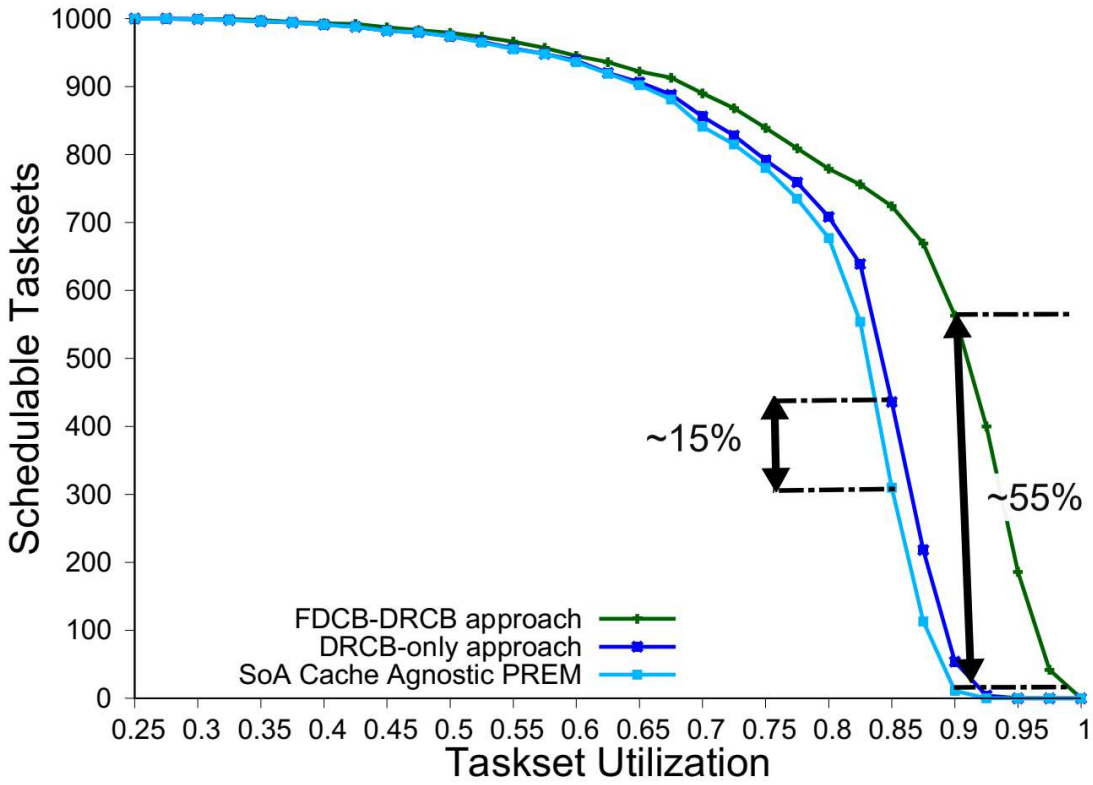
$$\underbrace{C_{i,j}}_{\text{WCET of E\_\{i,j\}}} = (\underbrace{|WB^{tot}_{i,j}|}_{\text{Total write-backs during the execution of E\_\{i,j\}}} + \underbrace{|ECB^{P}_{i,j}|}_{\text{Total prefetches during the execution of E\_\{i,j\}}}) \times \underbrace{d_{mem}}_{\text{Worst-case time to load one block from main memory}} + \underbrace{C^{e}_{i,j}}_{\text{Length of Execution Phase of E\_\{i,j\}}}$$

$$\underbrace{C_i}_{\text{WCET of } \tau_i} = \sum_{j=0}^{N_i-1} C_{i,j} \qquad \underbrace{R_i^{k+1}}_{\text{WCRT of } \tau_i} = B_i + C_i + \sum_{\forall h \in hp(i)} \left\lceil \frac{R_i^k}{T_h} \right\rceil C_h$$

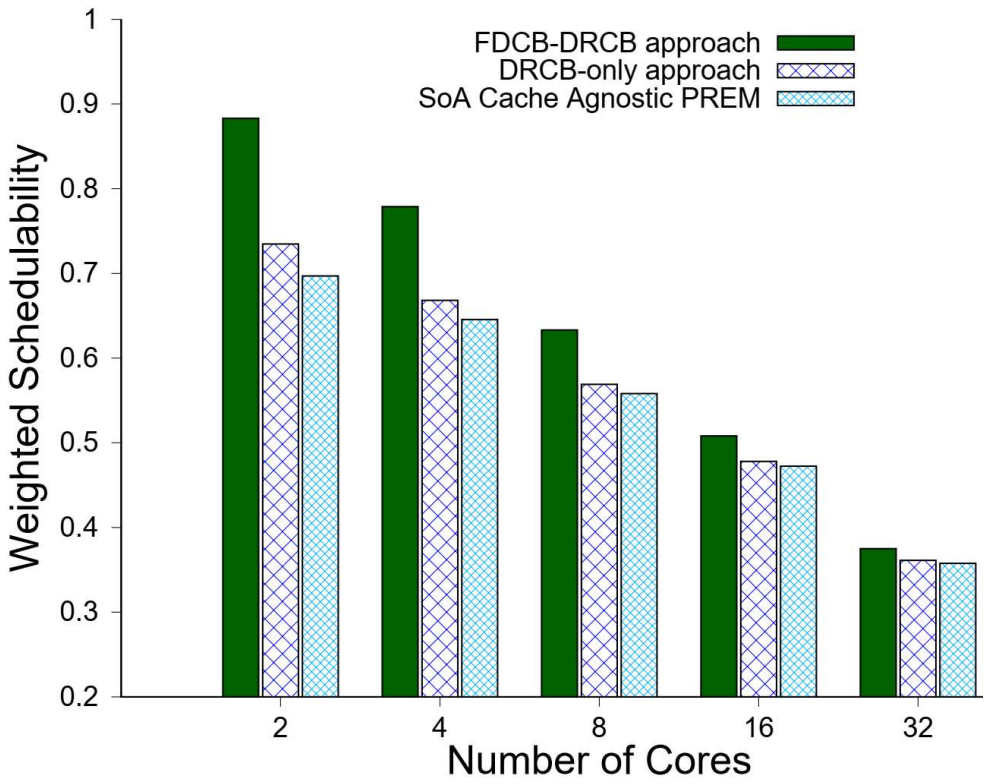
Experimental Evaluation: Experimental Setup and Taskset generation

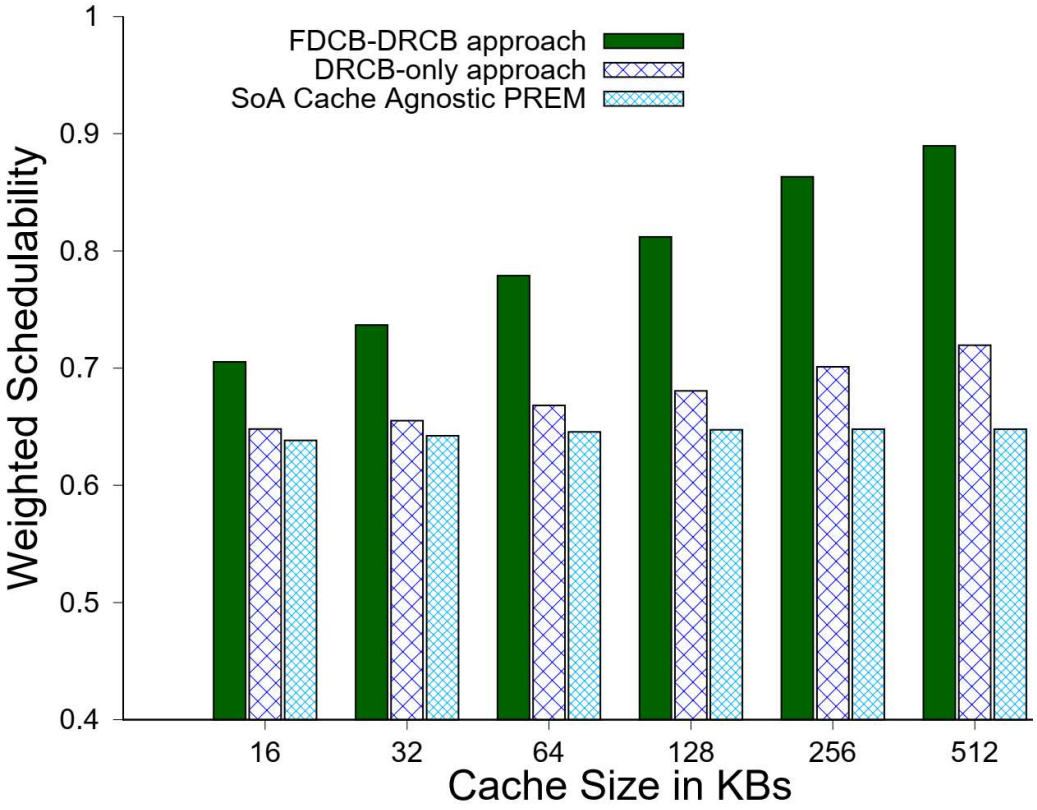
- We modeled a multicore platform with cores m=4, Last-level Cache = 64KB (2048 Cache sets, 32-byte blocks), Cache Prefetch/Write-back Penalty = 100 µSec
- Taskset size = 32, i.e., 8 tasks per core, Taskset Utilizations = UUnifast, Task periods = [5ms, 500ms], WCET = Utilization x Period, …
- 1000 synthetic tasksets per experimental point, compared SoA cache-agnostic PREM, DRCB-only approach and FDCB-DRCB approach.

Experimental Evaluation: Varying per Core Utilization

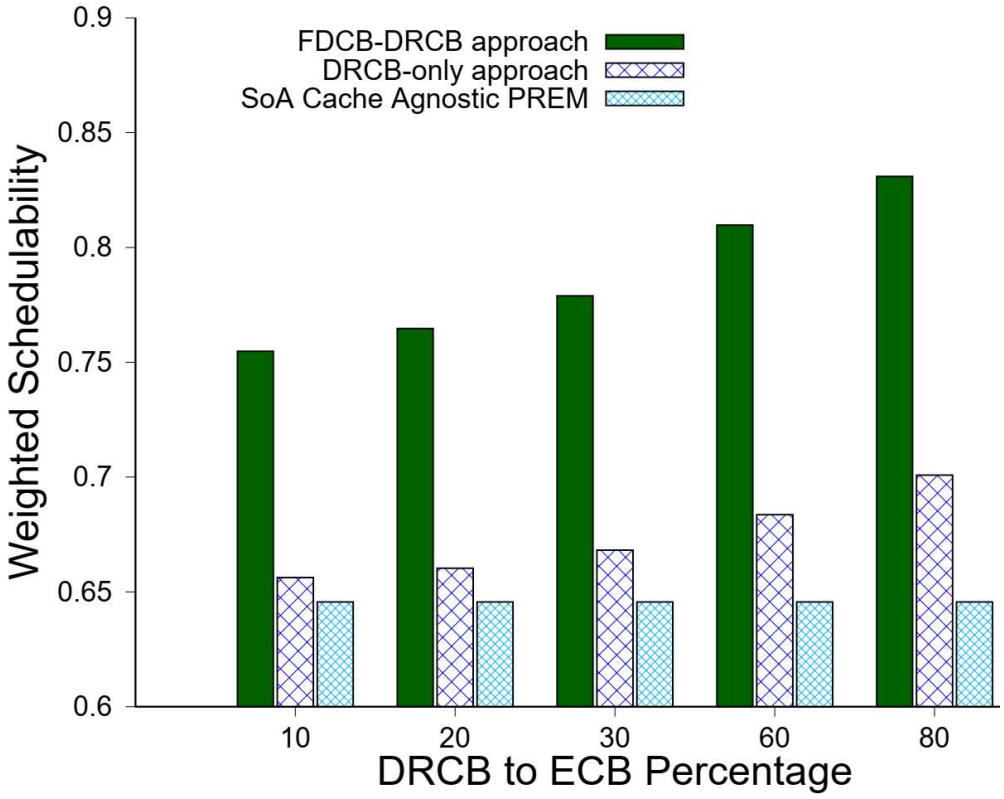


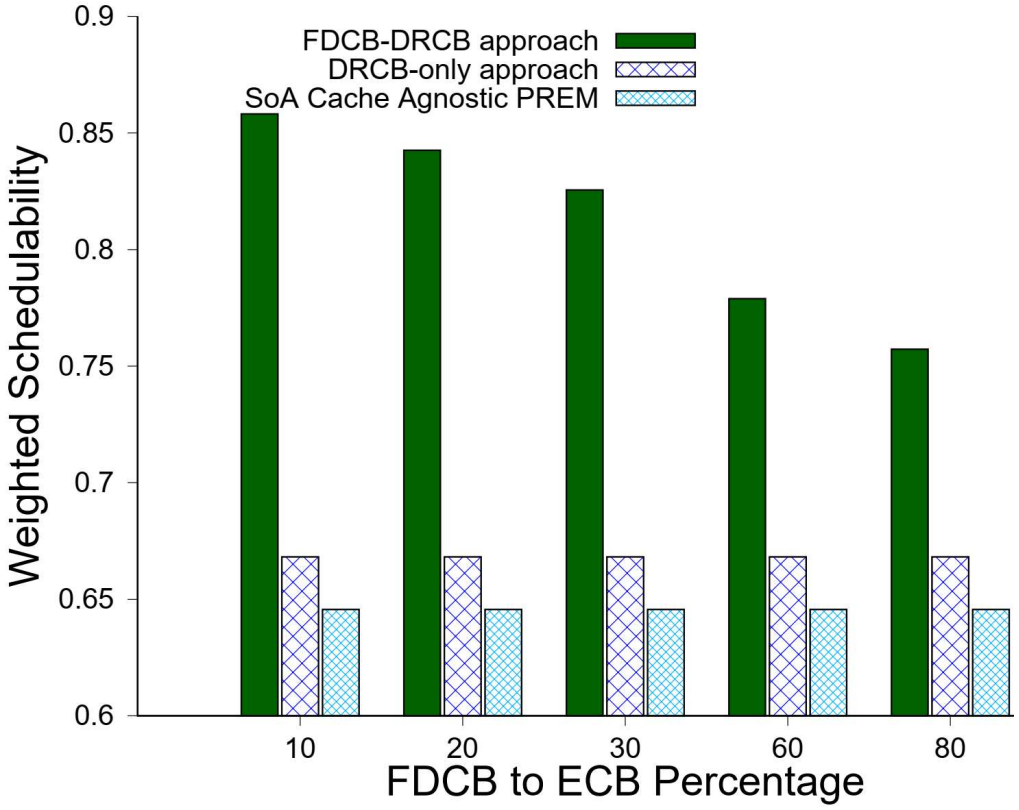
Experimental Evaluation: Varying number of Cores and Cache Size





Experimental Evaluation: Varying DRCB-ECB and FDCB-ECB percentage





Conclusion and Future Work

- Ported established cache-aware schedulability analysis to PREM
- Presented two approaches that tightly estimate cache line loads and write-backs
- DRCB-only approach exploits cache reuse among scheduling intervals to reduce the number of loads. The FDCB-DRCB approach improves on DRCB-only approach by carefully analyzing cache write-backs.
- Experimental evaluation shows that our approaches can achieve up to 55% better schedulability ratio.

- As future work, we aim to extend our analysis to multi-set approaches.
- We also plan to extend our analysis to consider inter-job cache reuse.

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Thank You ☺

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