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Challenges for Worst-Case Execution Time Analysis of Multi-Core Architectures

Abstract: In hard real-time systems, timely computation of outputs is as important as computing the correct output values. Worst-case execution time (WCET) analysis is a fundamental step in proving that all timing constraints of an application are met. Given a program and a microarchitecture, the task of WCET analysis is to determine an upper bound on the execution time of the program on the given microarchitecture under all possible program inputs. While this task is in general undecidable, it can be solved approximatively with sound abstractions.

Current microarchitectural developments make WCET analysis increasingly difficult: contemporary processor architectures employ deep pipelines, branch predictors, and caches to improve performance. Further, multicore processors share buses, caches, and other resources, introducing interference between logically-independent programs.

I will discuss three challenges arising from these developments, and approaches to overcome these challenges:

1) Modeling challenge: How do we construct sound models of complex hardware for timing analysis?

2) Analysis challenge: Given timing models of a microarchitecture, how to precisely and efficiently bound the WCET? What kind of properties do the models need to have to permit efficient analysis?

3) Design challenge: How should microarchitectures be constructed to enable precise and efficient WCET analysis without sacrificing average-case performance?