

Title of the Talk:


Design of On-Chip Cores and Sensors to Improve Embedded System Reliability

Summary:

This talk discusses recent research that has been carried out at the Catholic University - PUCRS dealing to enhance the reliability of System-on-Chip (SoC) devoted to critical embedded real-time applications. The goal of this talk is twofold:

(a) It describes the development of an intellectual property (IP) core to monitor embedded software activity. In this sense, an IP core has been developed to check two types of software activities: first, the IP core monitors the “*task scheduling process*” carried out by the operating system (OS) kernel. Second, the IP core monitors the “*worst-case execution time (WCET)*” of embedded applications running under the OS control. In both cases, the monitoring deals with on-line detection of control-flow and/or timing errors, on the field.

(b) Secondly, this talk addresses the development of on-chip sensors to monitor three issues: first, on-chip sensor is used to detect dynamic resistive open defects in nano-SRAMs; second, a dedicated sensor is used to monitor aging effects that reduce very-deep submicron (VDSM) SRAMs lifetime. A modified version of this sensor has been developed to monitor aging of logic implemented in field programmable gate arrays (FPGAs). Third, on-chip sensor is used to detect single-event upsets (SEUs) in SRAMs exposed to radiation. In this case, on-chip sensor is coupled with parity code to allow error detection and correction of radiation-induced soft errors in SRAM cells.

	<p>Fabian Vargas obtained his Ph.D. Degree in Microelectronics from the <i>Institut National Polytechnique de Grenoble</i> (INPG), France, in 1995. At present, he is Full Professor at the Catholic University (PUCRS) in Porto Alegre, Brazil. His main research domains involve the HW-SW co-design and test of system-on-chip (SoC) for critical applications; system-level design and methodologies for radiation and electromagnetic compatibility; and the embedded sensor design for characterization, reliability and speed binning.</p> <p>Among several activities, Prof. Vargas has served as Technical Committee Member or Guest-Editor in many IEEE-sponsored conferences and journals. He holds 6 BR and international patents, co-authored a book and published over 200 refereed papers. Prof. Vargas is associate researcher of the BR National Science Foundation since 1996. He co-founded the IEEE-Computer Society Latin American Test Technology Technical Council (LA-TTTC) in 1997 and the IEEE Latin American Test Workshop (LATW) in 2000. Prof. Vargas received the Meritorious Service Award of the IEEE Computer Society for providing significant services as chair of the IEEE Latin American Regional TTTC Group for six years and for chairing the LATW for several times. Prof. Vargas is a Golden Core Member of the IEEE Computer Society.</p>
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